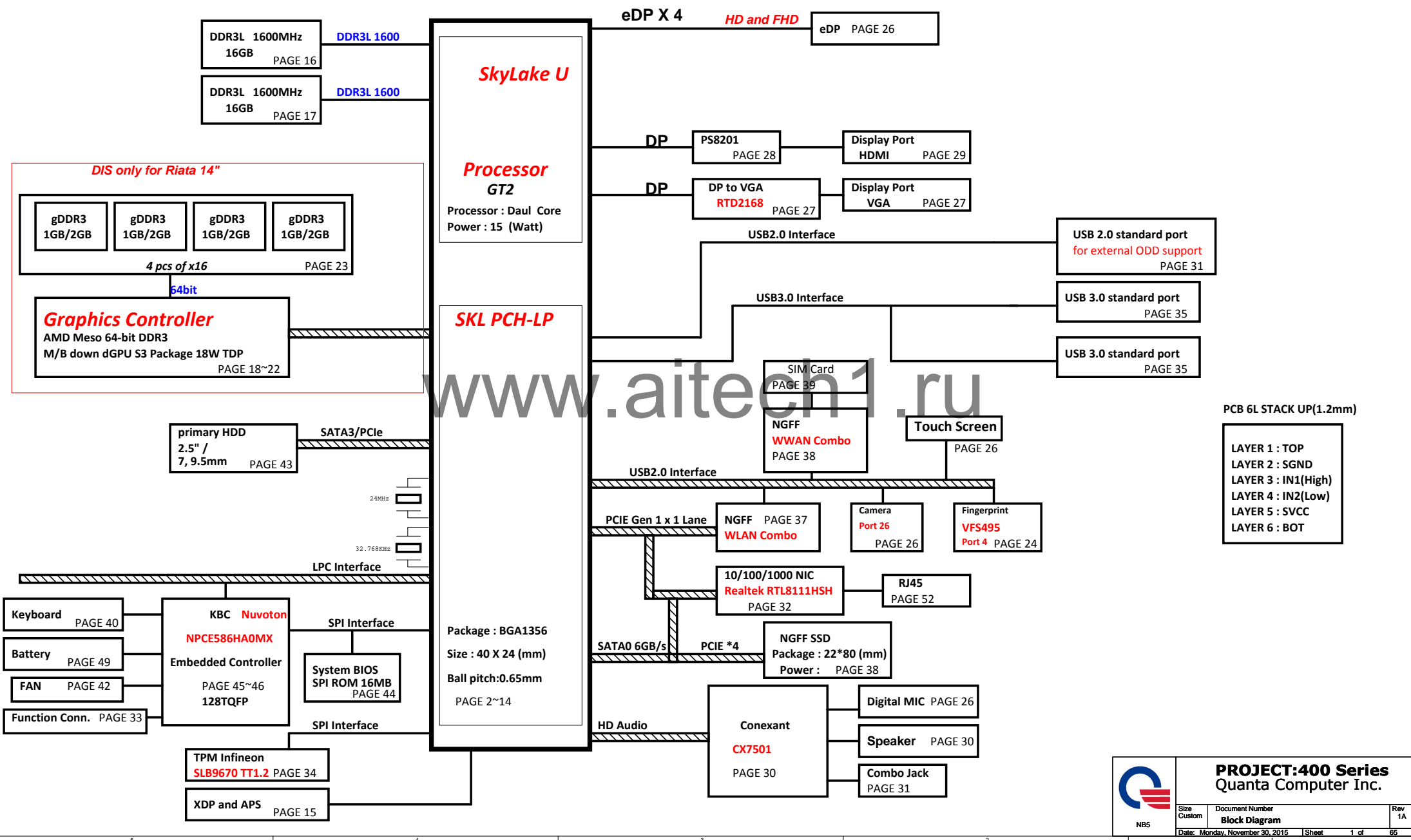
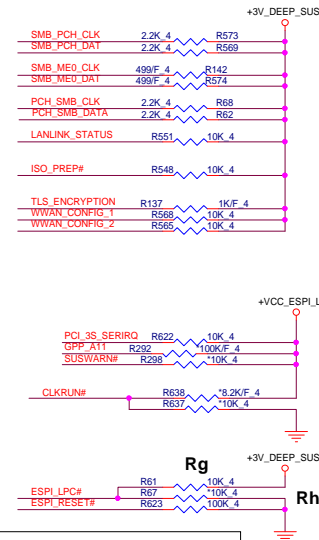


# Royal 13"/Riata 14" SkyLake -U (UMA/DIS) Schematics

01

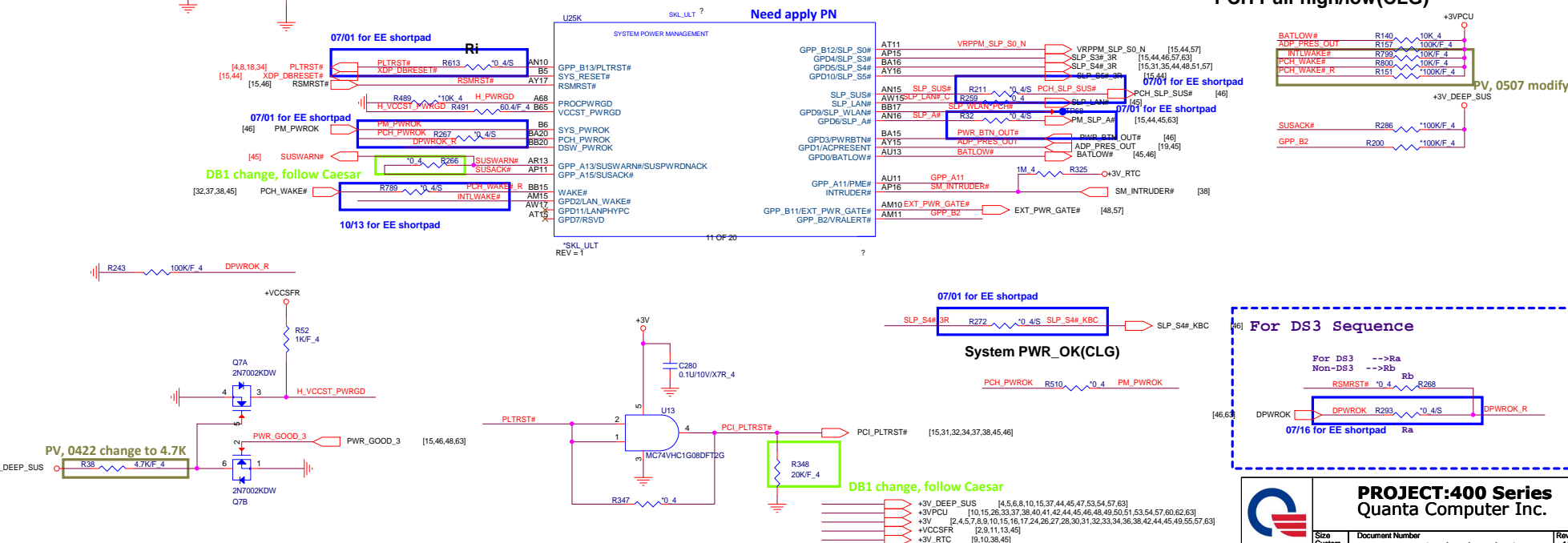


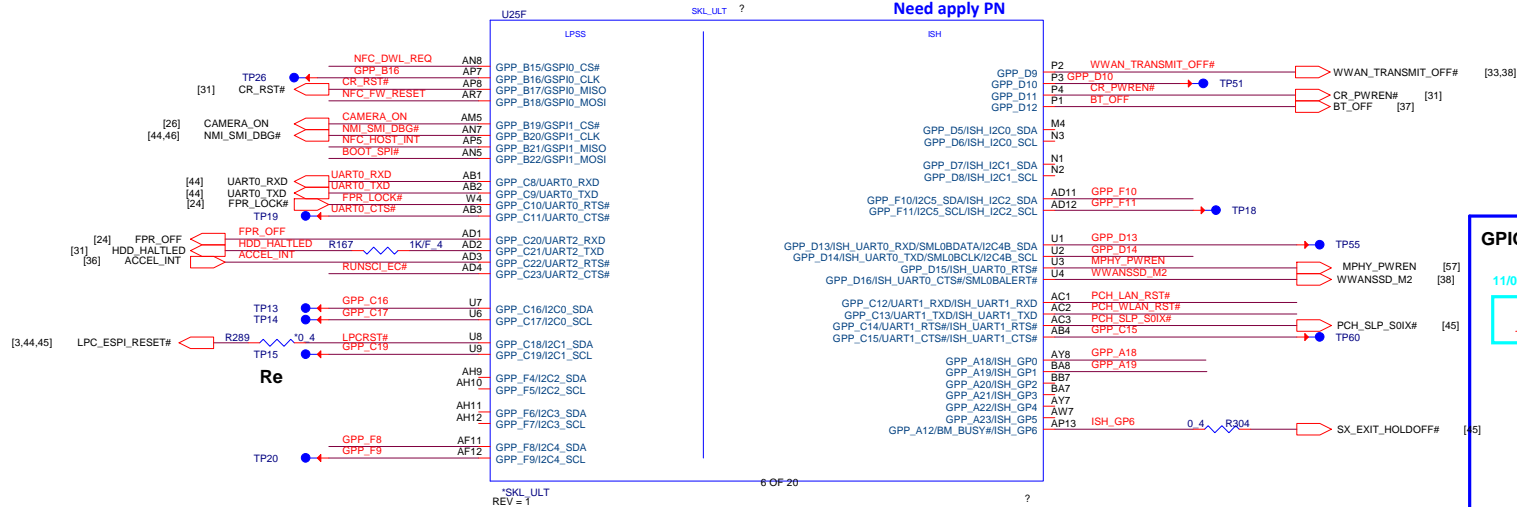




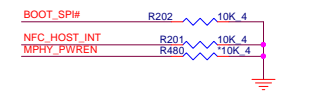
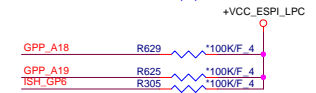
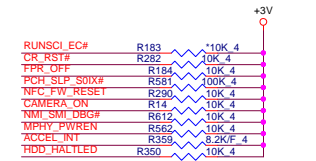
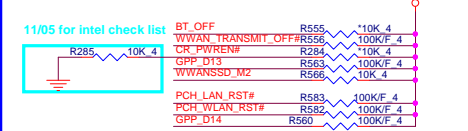
		LPC MODE	ESPI MODE
R620	<b>Ra</b>	15Ω	15Ω
R621	<b>Rb</b>	15Ω	15Ω
R633	<b>Rc</b>	15Ω	15Ω
R634	<b>Rd</b>	15Ω	15Ω
R289	<b>Re</b>	INSTAL	UNINSTAL
R636	<b>Rf</b>	UNINSTAL	INSTAL
R64	<b>Rg</b>	UNINSTAL	INSTAL
R67	<b>Rh</b>	INSTAL	UNINSTAL
R623	<b>Ri</b>	INSTAL	UNINSTAL
R183	<b>Rj</b>	INSTAL	UNINSTAL

### PCH Pull-high/low(CLG)

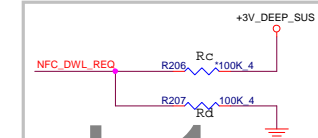




### GPIO Pull-up/Pull-down(CLG)



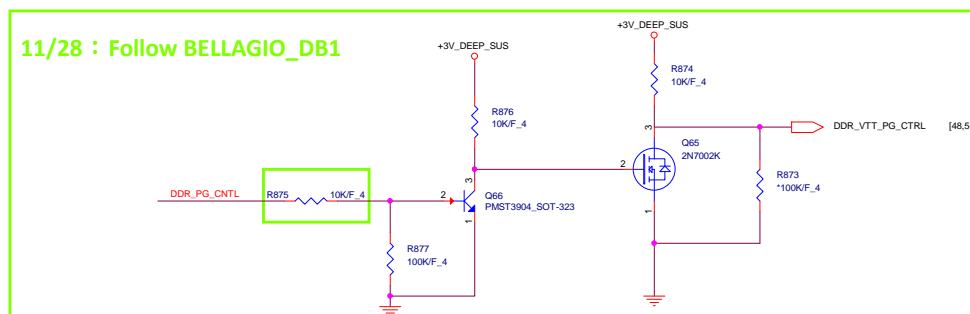
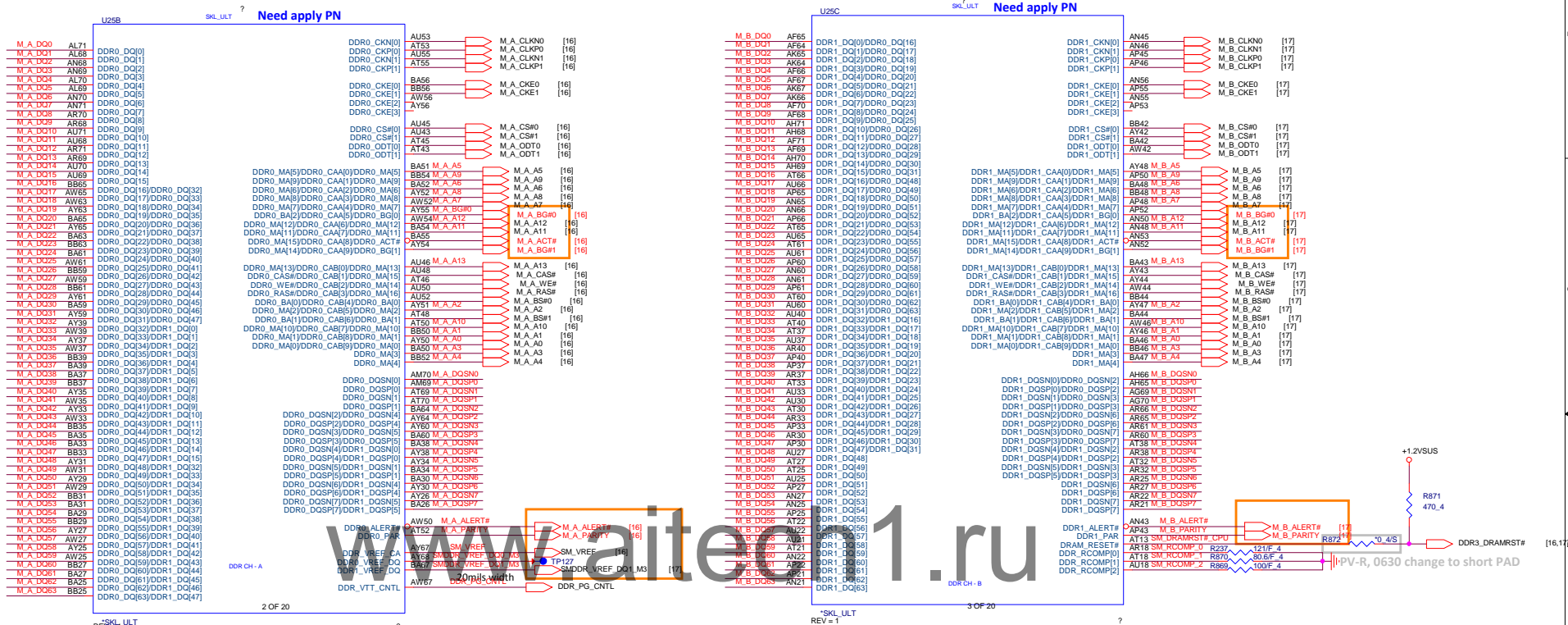
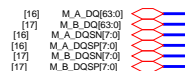
PV-R, 0701 for NFC\_DWL\_REQ WWAN & TS TABLE

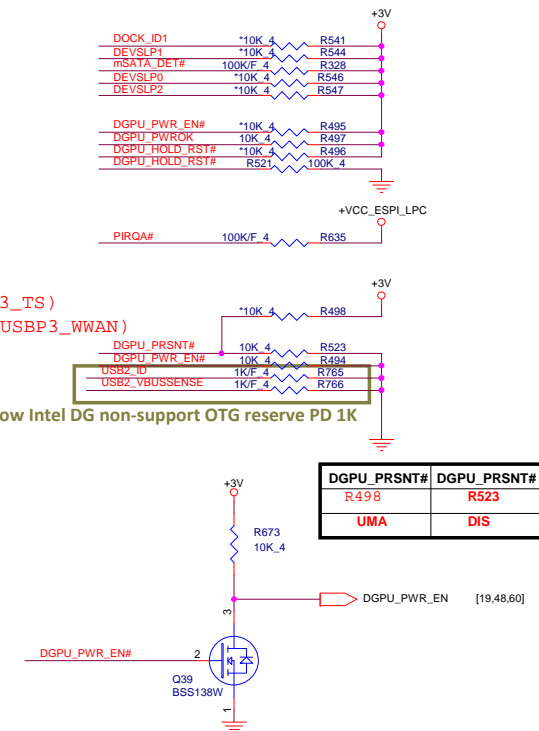


WWAN & TS TABLE		
	WWAN MODE	TS MODE
R206	INSTAL	UNINSTAL
R207	UNINSTAL	INSTAL

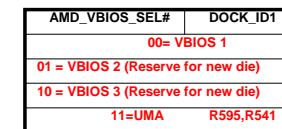



[illegible][illegible]





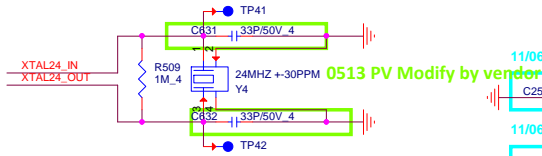
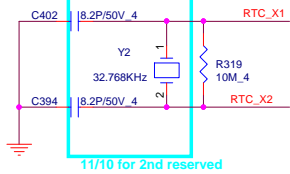
DGPU_PRSENT#	DGPU_PRSENT#
R498	R523
UMA	DIS



 <b>NBS</b>	<b>PROJECT:400 Series</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>08 – SKYLAKE (HDA)</b>	Rev 1A
	Date: Monday, November 30, 2015	Sheet 8 of	65

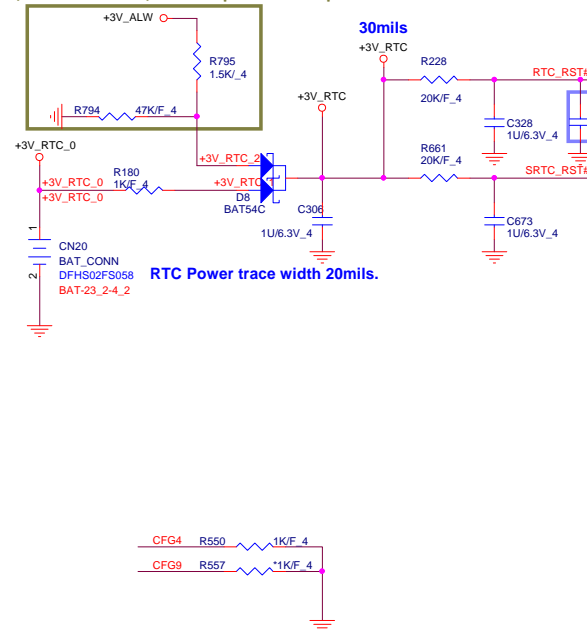
TBT

## RTC Clock 32.768KHz



## RTC Circuitry(RTC)

PV, 0413 add R795, R794 to prevent RTC power over +3.2V



+VCCSFR [2,3,11,13,45]  
+1.0V\_DEEP\_SUS [10,15,52,53,54,57]  
+3V [2,3,4,5,7,8,10,15,16,17,24,26,27,28,30,31,32,33,34,36,38,42,44,45,49,55,57,63]

Cardreader

LAN

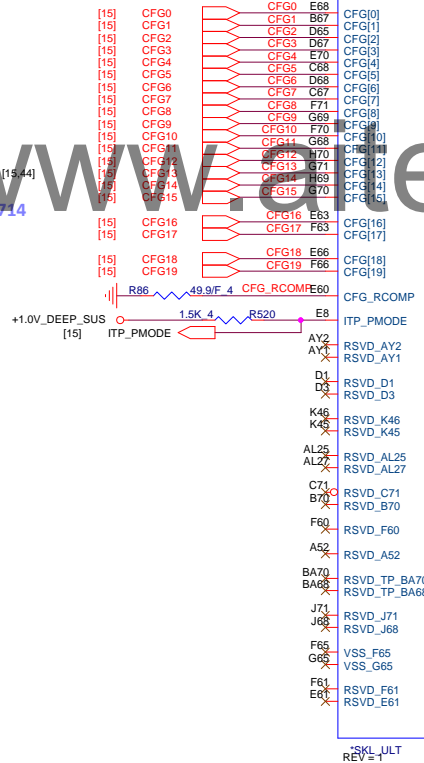
WLAN

dGPU

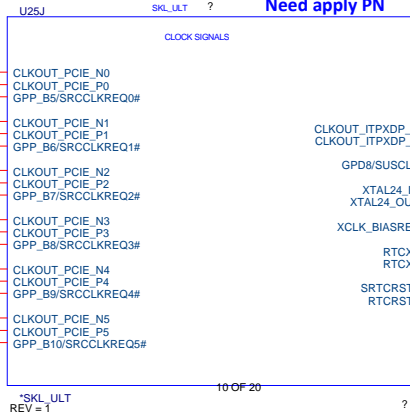
11/06 for RF reserved

11/06 for RF reserved

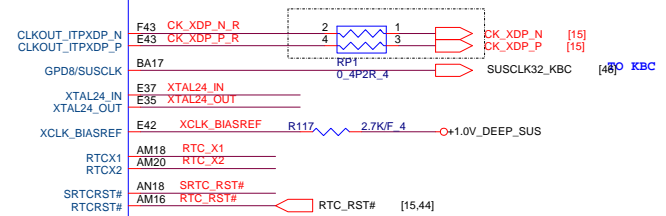
CFG0-19 need Reserve TP



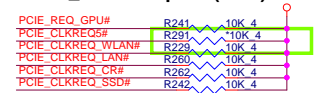
Need apply PN



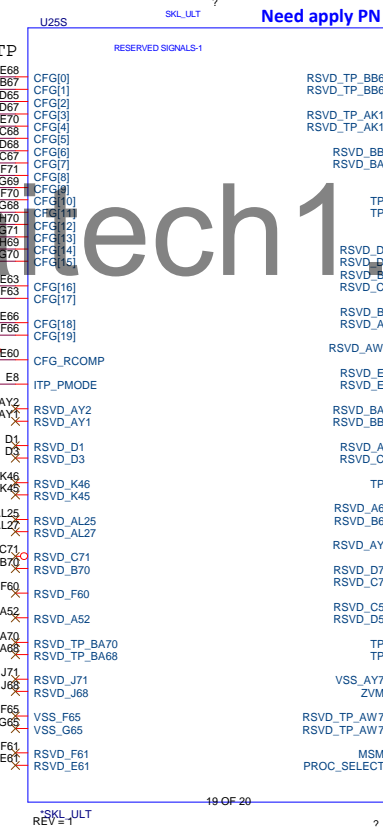
RPl install for XDP



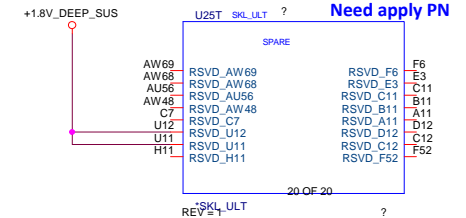
CLK\_REQ/Strap Pin(CLG)



Need apply PN

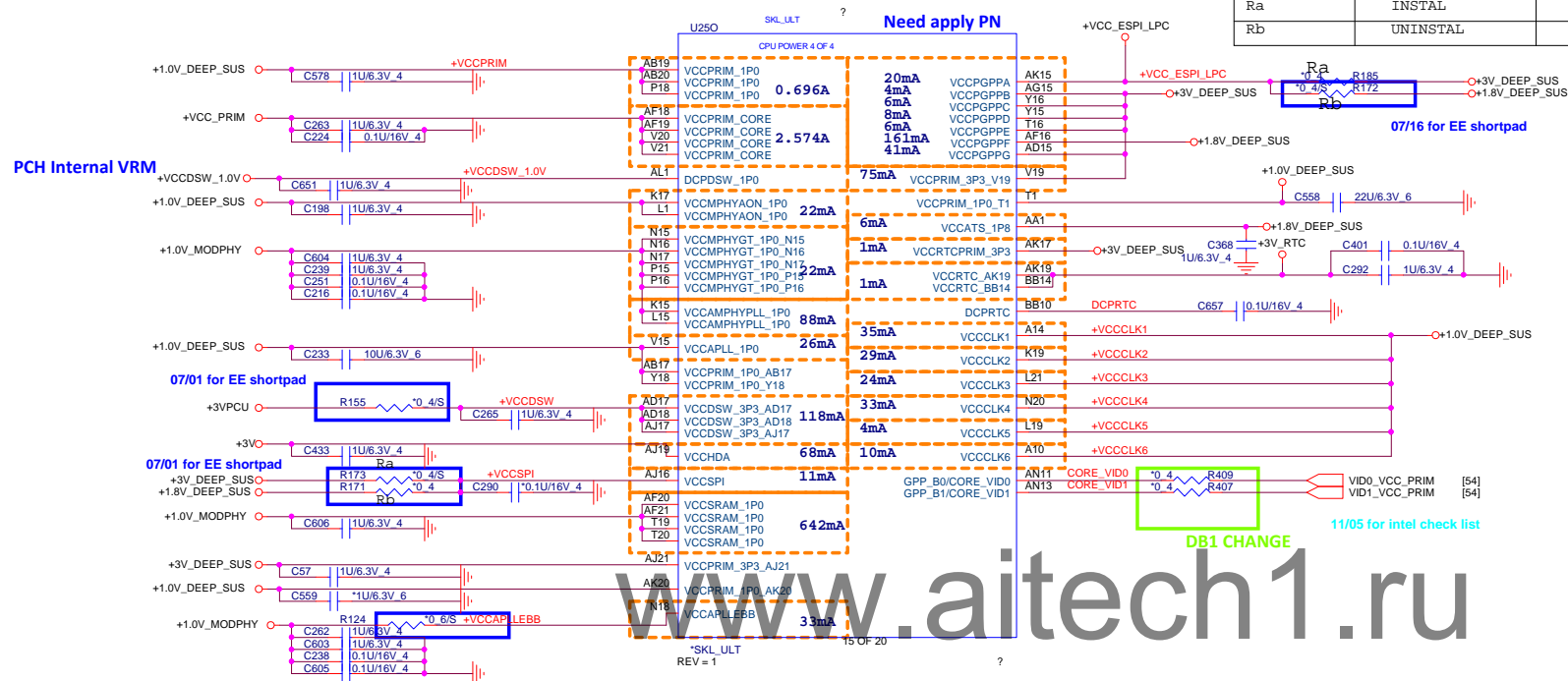


Need apply PN



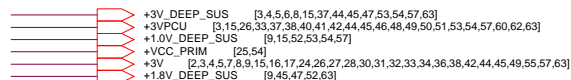
**PROJECT:400 Series**  
**Quanta Computer Inc.**

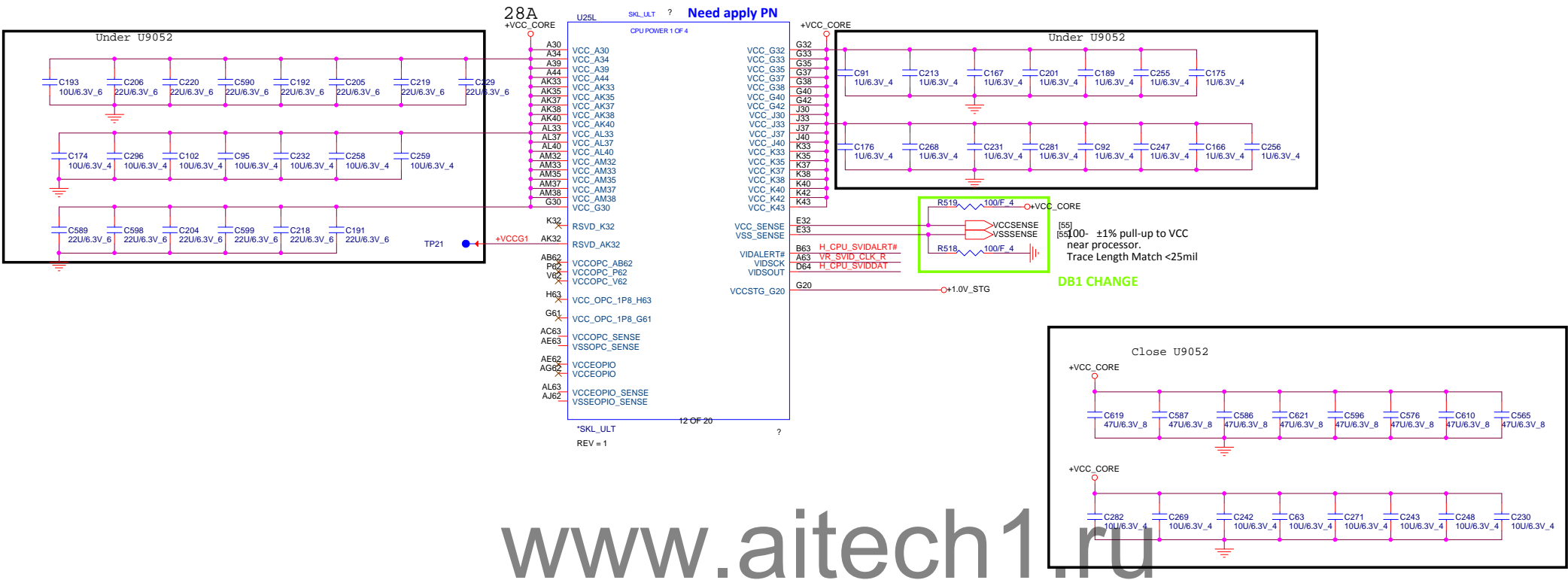
Size Custom	Document Number <b>09 - SKYLAKE (CLK/RSV/RTC)</b>	Rev 1A
Date: Monday, November 30, 2015	Sheet	9 of 65



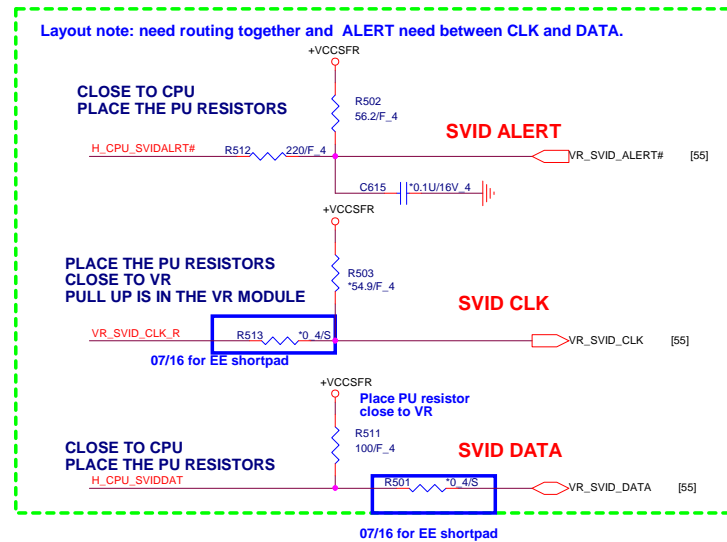
LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
Ra	INSTAL	UNINSTAL
Rb	UNINSTAL	INSTAL

LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
Ra	INSTAL	UNINSTAL
Rb	UNINSTAL	INSTAL

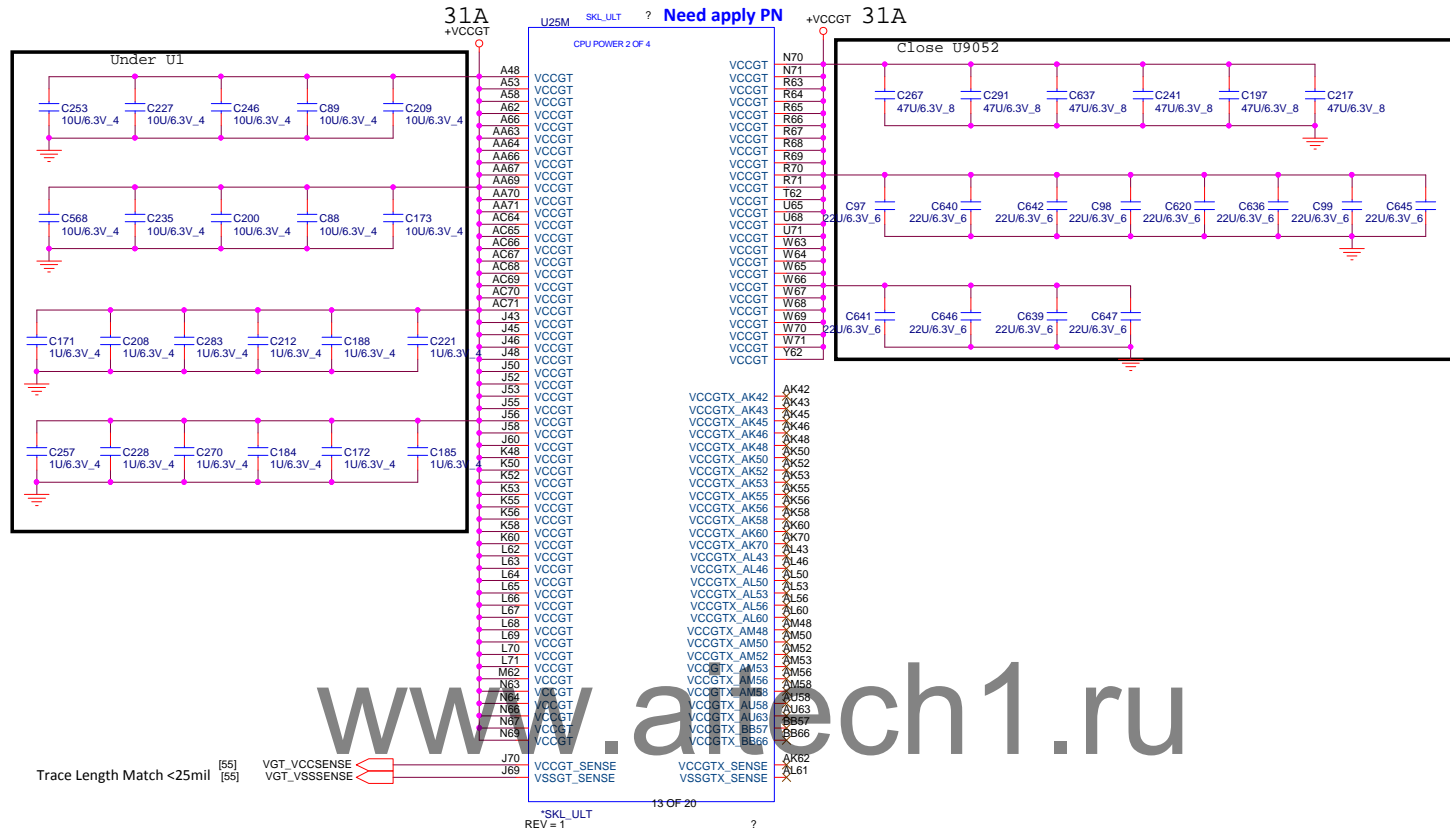




Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTx</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_1P8</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

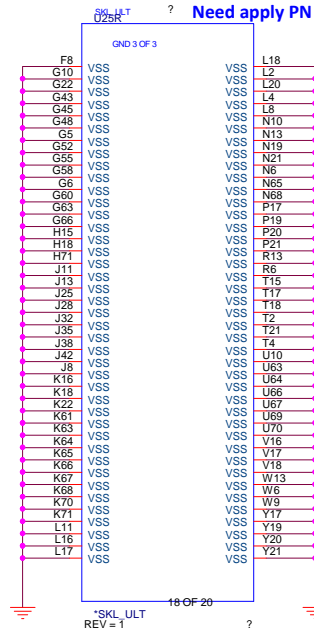
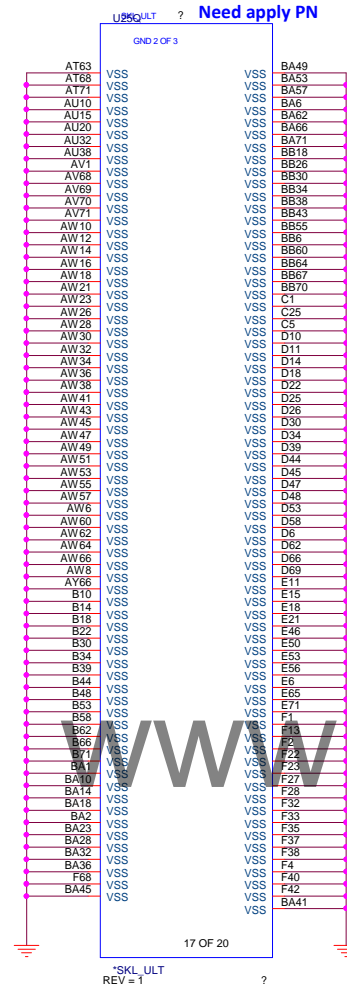
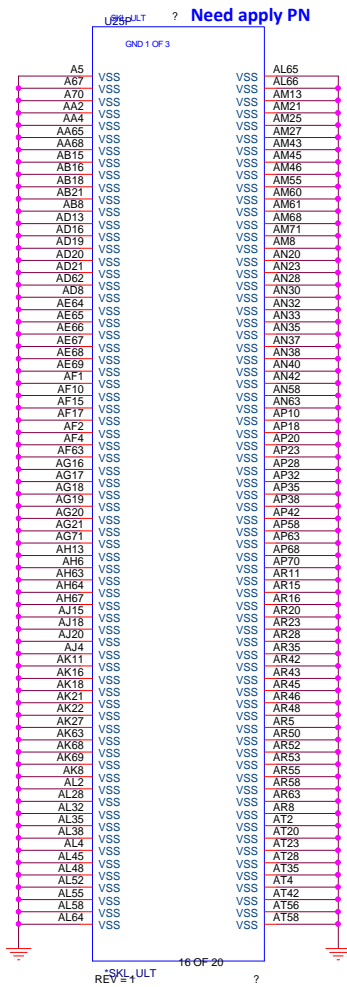




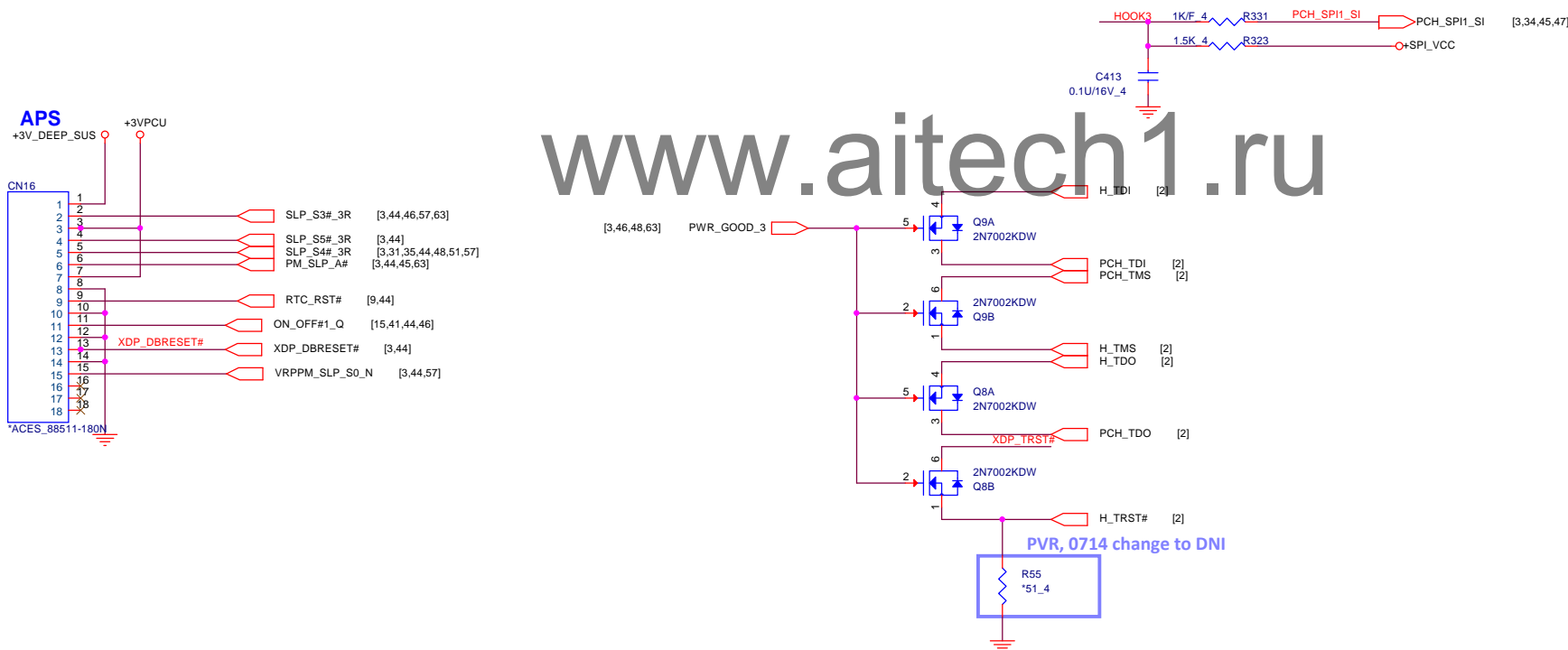
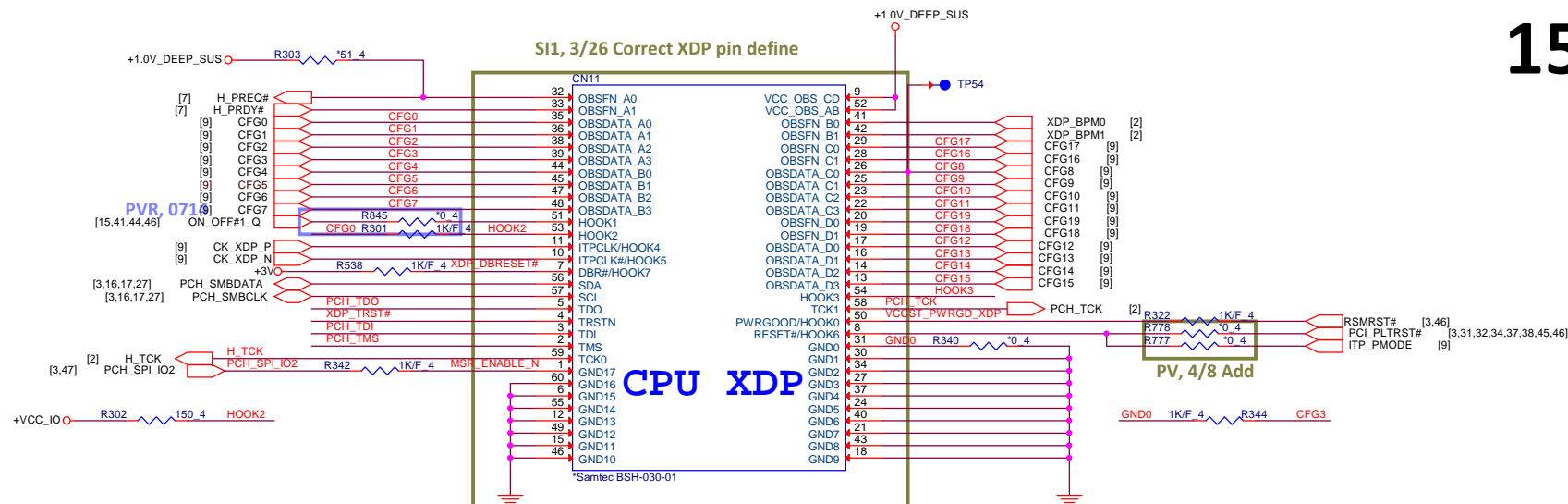


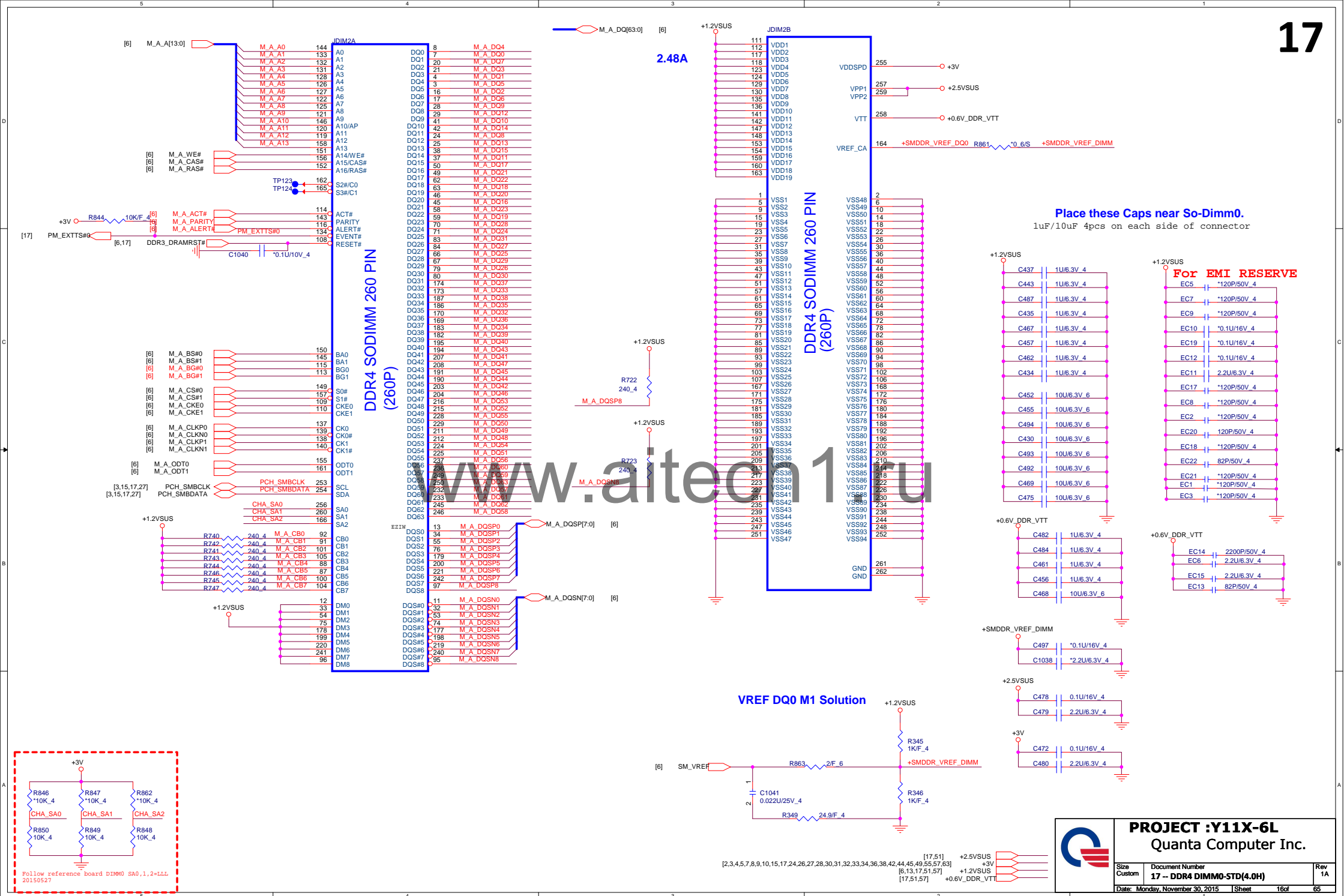






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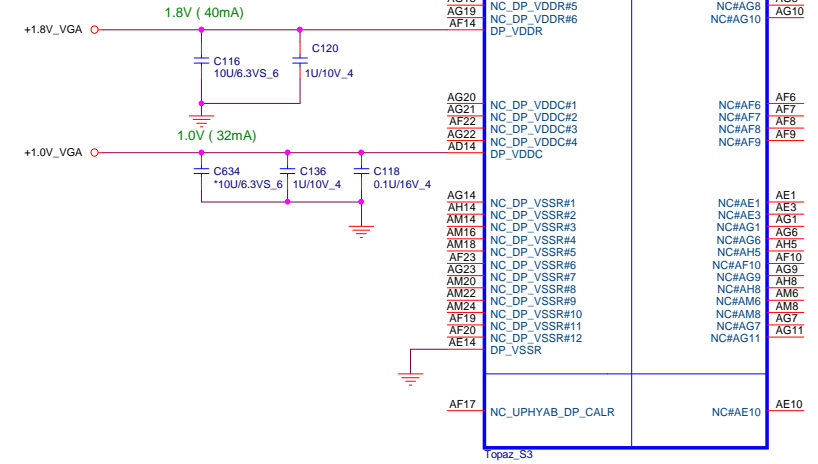




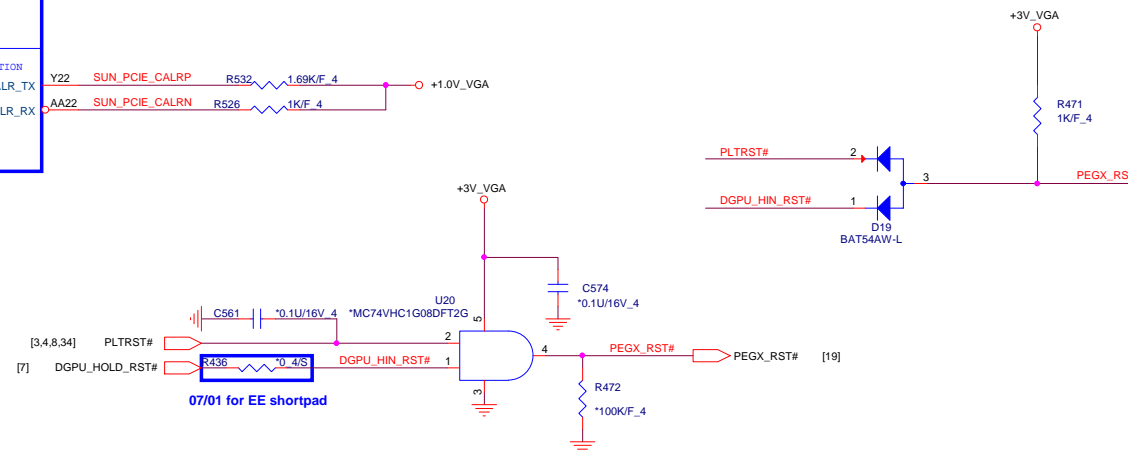


Platform	Type	P/N
Carrizo	Gen 3	CH4222K9B04
Carrizo-L	Gen 1/Gen 2	CH4102K1B03


9/2: CZ use 0.22u(Gen 3) ; CZ-L use 0.1u(Gen 2)

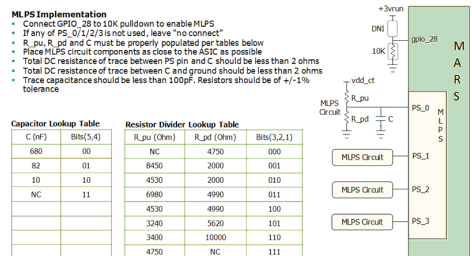





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[19,21,60] +3V\_VGA  
 [19,21,58,60] +1.8V\_VGA  
 [21,60] +1.0V\_VGA

 NB5	<b>PROJECT:400 Series</b>		
	<b>Quanta Computer Inc.</b>		
	Size	Document Number	Rev
	<b>18 – Meso_S3_PCIE/DP POWER</b>		<b>1A</b>
Date:	Monday, November 30, 2015   Sheet 18 of 65		



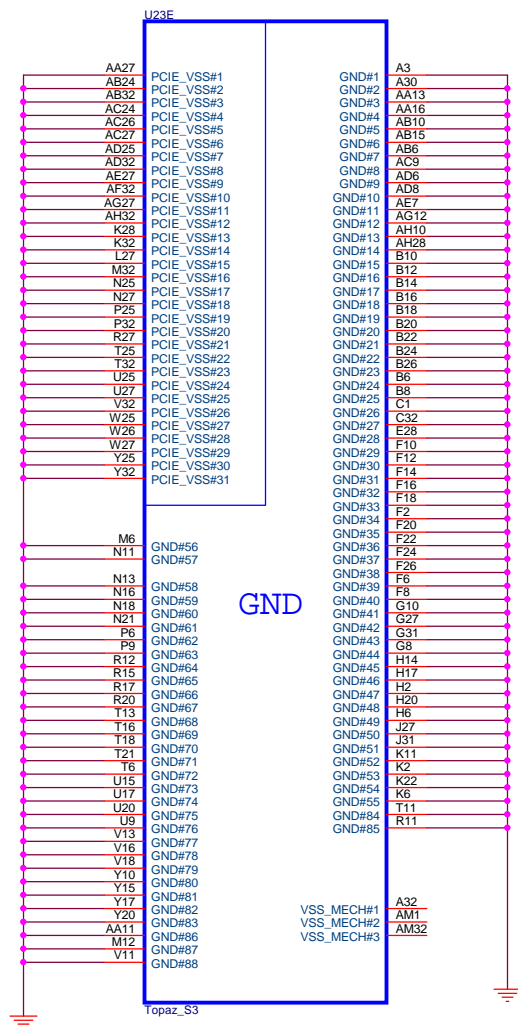
Capacitor Lookup Table		Resistor Divider Lookup Table			
C (pF)	Bin(5,4)	R_p (Ohm)	R_d (Ohm)	Bin(3,2,1)	
680	00	NC	4750	000	
82	01	8450	2000	001	
10	10	4530	2000	010	
NC	11	6980	4990	011	
		4530	4990	100	
		3240	5620	101	
		3400	10000	110	
		4750	NC	111	

BITS => BIT0		Bit	Strap Name	Description
PS0	=> 11001	PS_0[01]	ROM_CONFIG[0]	IF STRAP BIOS.ROM.EN = 1, ROM_CONFIG[0:0] define the ROM type.
PS1	=> 11000	PS_0[02]	ROM_CONFIG[1]	IF STRAP BIOS.ROM.EN = 0, ROM_CONFIG[0:1] define the primary memory aperture size. Primary Memory Aperture Size 209
PS2	=> 11000	PS_0[03]	ROM_CONFIG[2]	Reserved for internal use only. Must be 1 at reset.
PS3	=> 11000	PS_0[04]	N/A	Reserved.
		PS_0[05]	N/A	Reserved.
				PCIe GEN3 capability

		GEN3_EN_A	0 = PCIe GEN3 is not supported 1 = PCIe GEN3 is supported
	PS_1[12]	STRAP_BIF_CLK_PM_EN	Determines whether or not the PCIe reference clock power management capability is report in the PCI configuration space (otherwise known as CLKREQ#) 0 = The CLKREQ# power management capability is disabled 1 = The CLKREQ# power management capability is enabled
	PS_1[13]	N/A	Reserved for internal use only. Must be 0 at reset.
	PS_1[14]	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-half swing mode 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled
	PS_1[15]	STRAP_TX_DEEMPH_EN	PCI EXPRESS# transmitter, de-emphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.
	PS_2[11]	N/A	Reserved.
	PS_2[12]	N/A	Reserved.
	PS_2[13]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.
	PS_2[14]	N/A	Reserved.
	PS_2[15]	N/A	Reserved.
	PS_3[11]	BOARD_CONFIG[0]	Board configuration related strapping, such as for memory
	PS_3[12]	BOARD_CONFIG[1]	
	PS_3[13]	BOARD_CONFIG[2]	
	PS_3[14]	N/A	Reserved.
	PS_3[15]	N/A	Reserved.

PS_3[3:1]	Vendor	Type	Vendor P/N	QCI P/N	PU	PD
000	Samsung- Q die	128Mx16 *4, 1Ghz	K4W2G1646Q-BCLIA	AKDSMGST508/AKDSMGST509	NC	4.75K
001	Samsung- E die	256Mx16 *4, 1Ghz	K4W4G1646E-BCLIA	AKDSPGD7500/AKDSPGD7501	8.45K	2K
010	Hynix- Huma F die	128Mx16 *4, 1Ghz	H5TCZG63FFR-11C	AKDSMDZTW02/AKDSMDZTW03	4.53K	2K
011	Hynix- C(Polaris)	256Mx16 *4, 1Ghz	H5TC4G63CFR-N0C	AKDSPDZTW01/AKDSPDZTW02	6.98K	4.99K
100	Micron- K die	128Mx16 *4, 1Ghz	MT41J128M163T-093G:K	AKDSMGSTL16/AKDSMGSTL17	4.53K	4.99K
101	Micron- E die	256Mx16 *4, 1Ghz	MT41J256M16HA-093G:E	AKDSPS2TL00/AKDSPS2TL01	3.24K	5.62K
110	Nanya- I die	128Mx16 *4, 1Ghz	N75CB128M16FP-PL	AKDSNGSTF03/AKDSNGSTF04	3.4K	10K
111	Nanya- D die	256Mx16 *4, 1Ghz	N75CB256M16DP-FL	AKDSPGDTF02/AKDSPGDTF03	4.75K	NC
Vendor ID	VRAM density	Memo Multi-level Pin Straps				
00 = Samsung 01 = Hynix 10 = Micron 11 = Nanya	0=128Mx16 1=256Mx16	MLPS Bit: PS_3 mappings between the bit values and resistor values				





### CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS  
0= DO NOT INSTALL RESISTOR  
1= INSTALL 3K RESISTOR  
X = DESIGN DEPENDANT  
NA = NOT APPLICABLE

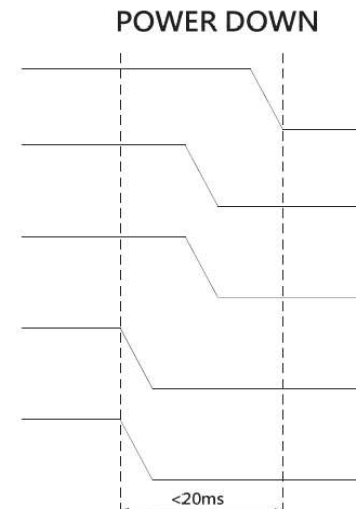
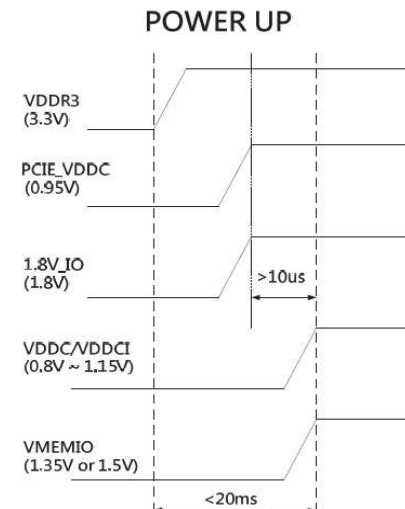
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/W/histler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	SEE DATABOOK FOR DETAIL SEE DATABOOK FOR DETAIL	0 0
RSVD	GENERICC	RESERVED	0

### NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

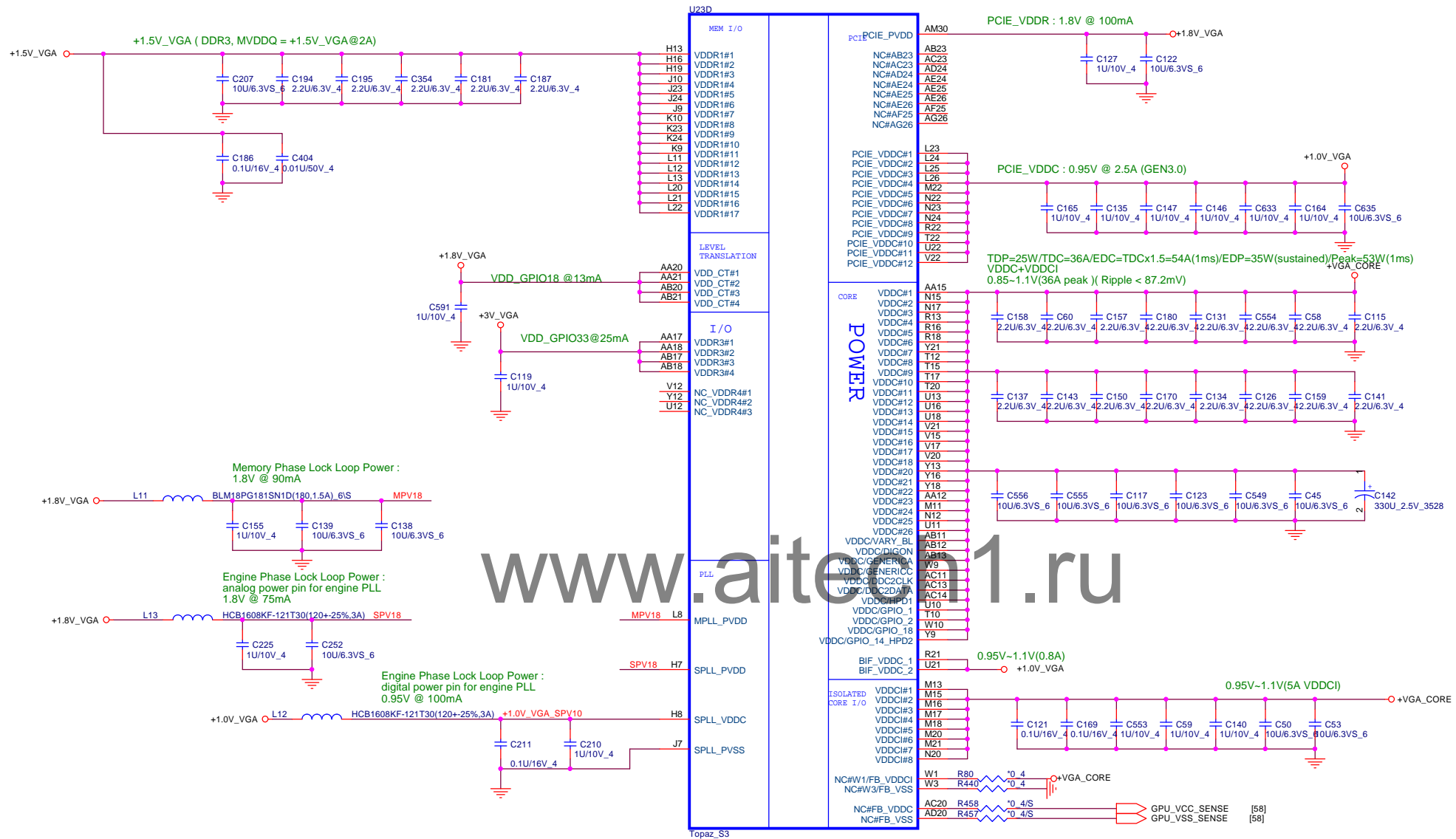
### POWER UP / POWER DOWN SEQUENCE



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Quanta Computer Inc.

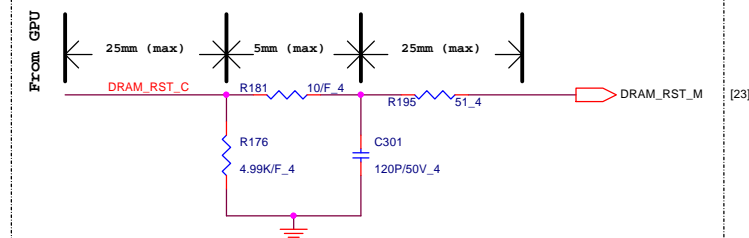
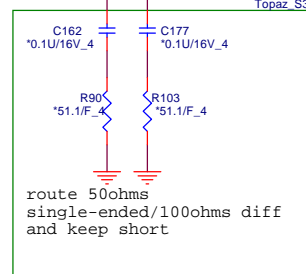
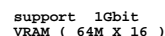
Size	Document Number	Rev
20	20 - Meso_S3_GND/LVDS/Strap	1A
Date:	Monday, November 30, 2015	Sheet 20 of 65





# PROJECT:400 Series Quanta Computer Inc.

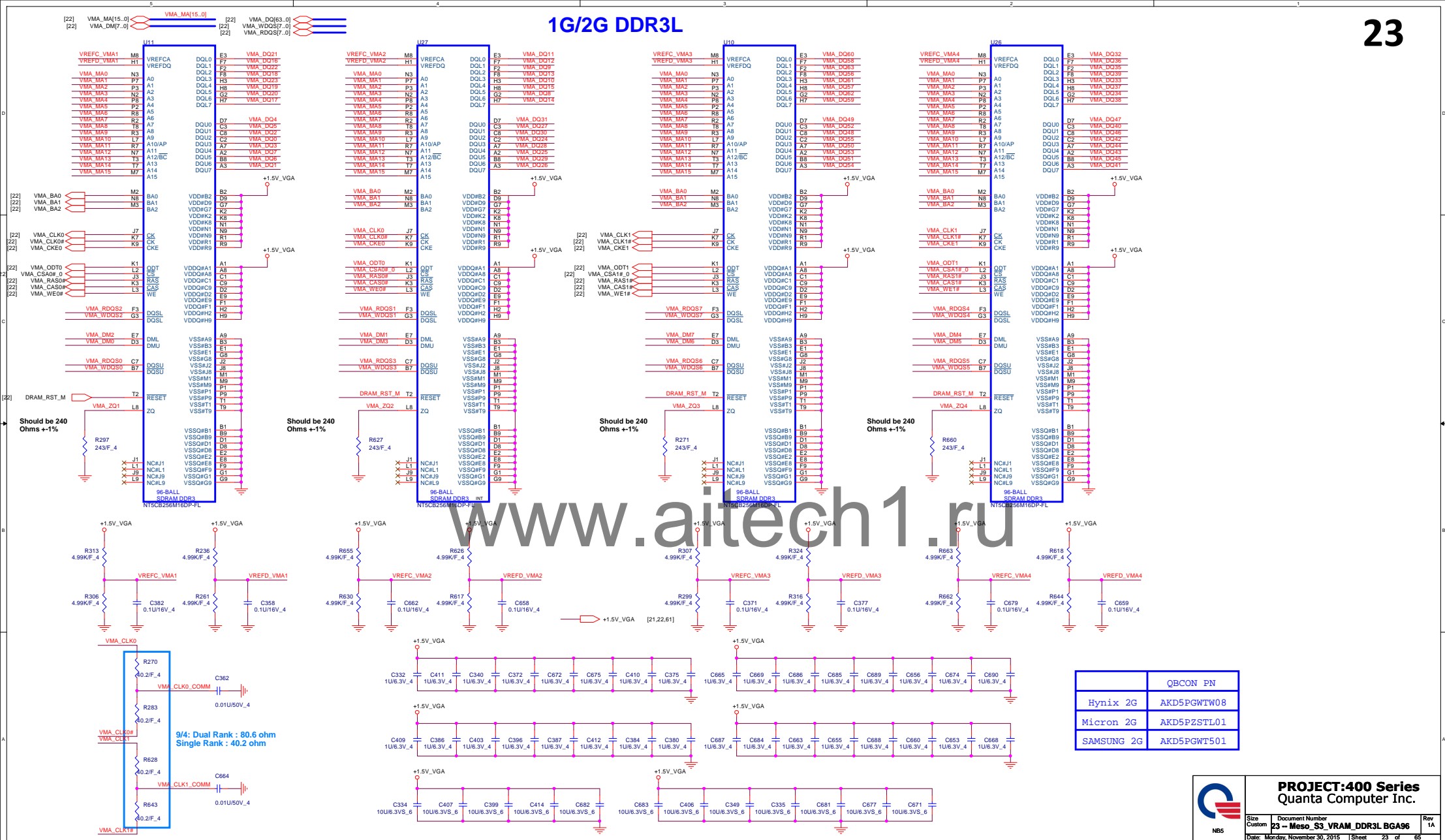
Size	Document Number	Rev
	<b>21 - Meso_S3_Power</b>	1A
Date:	Monday, November 30, 2015	Sheet 21 of 65



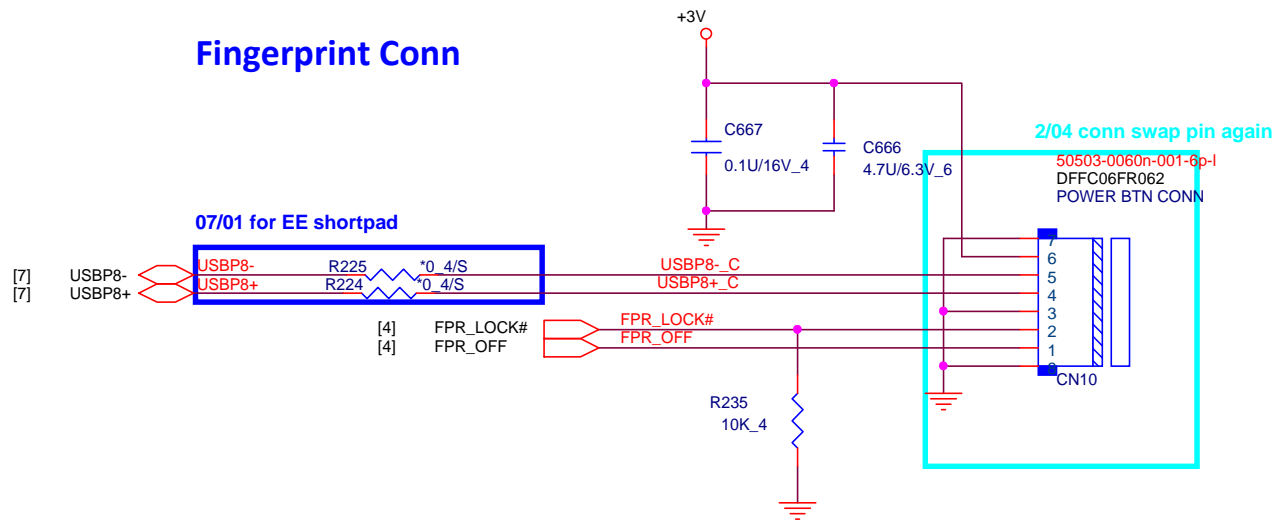
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM\_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

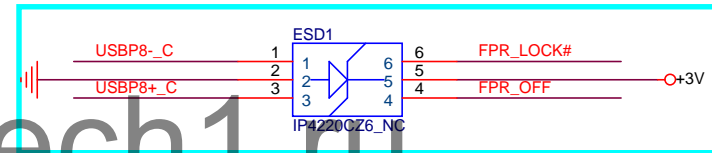
## 1G/2G DDR3L



## Fingerprint Conn



2/11 ESD1 swap pin



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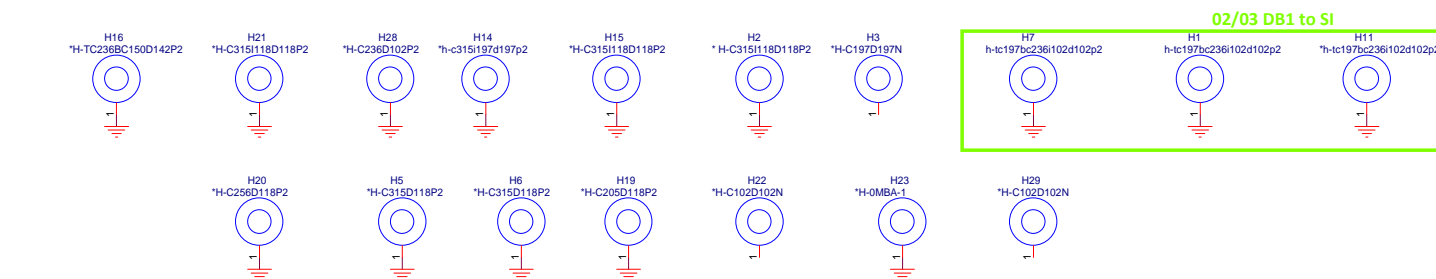
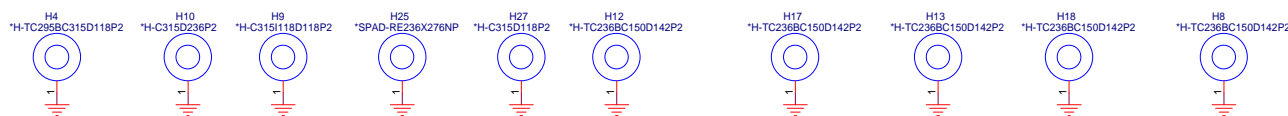
**PROJECT:400 Series**  
Quanta Computer Inc.

Size  
CustomDocument Number  
**24 -- FPR**Rev  
1A

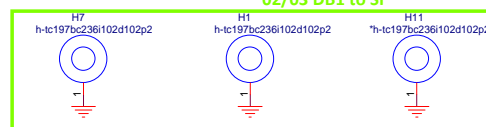
Date: Monday, November 30, 2015

Sheet 24 of 65

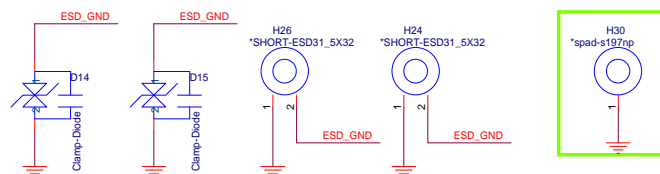
Hole



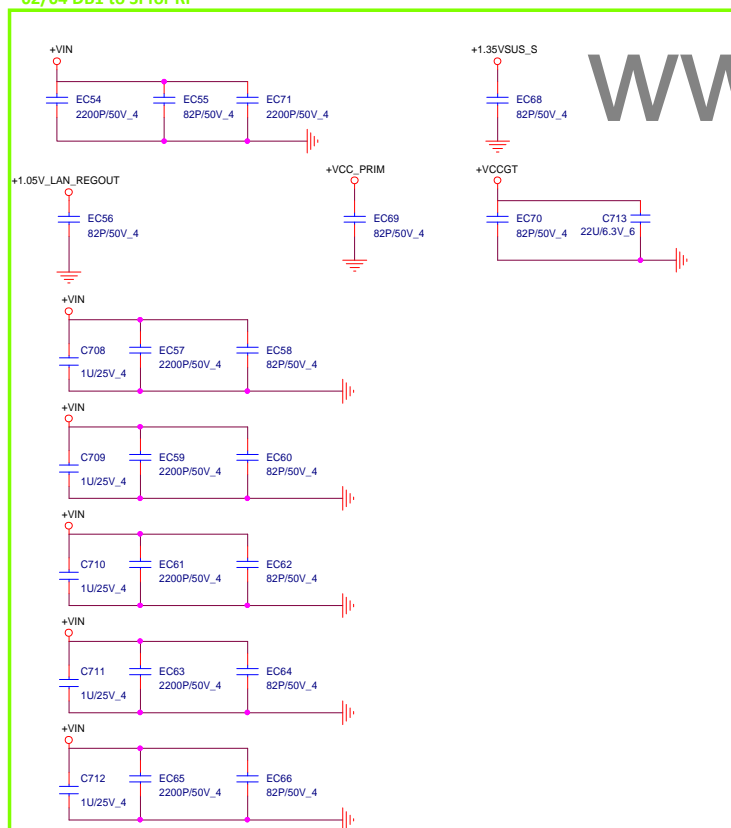
02/03 DB1 to SI



02/11 DB1 to SI



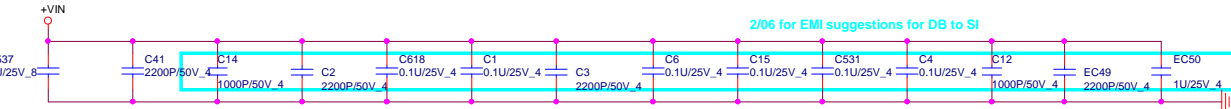
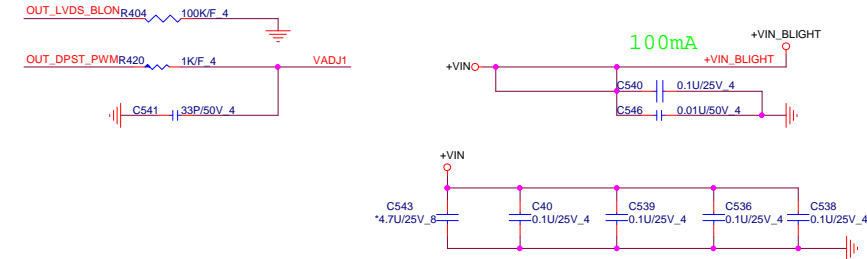
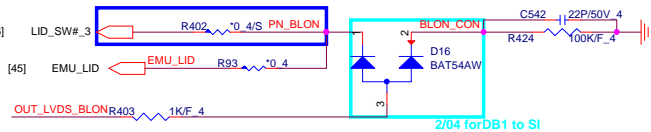
02/04 DB1 to SI for RF



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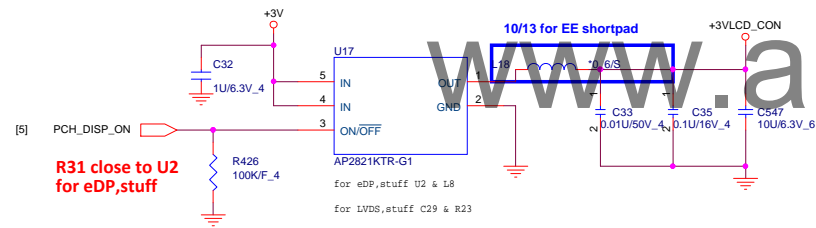
# LID Switch

07/01 for EE shortpad

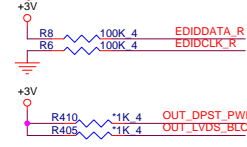


## For eDP

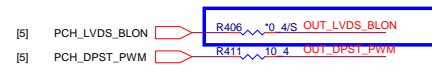
Close to LVDS connector



## For EDP Only: Reserved

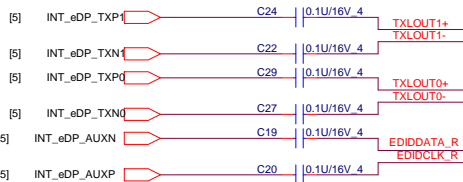
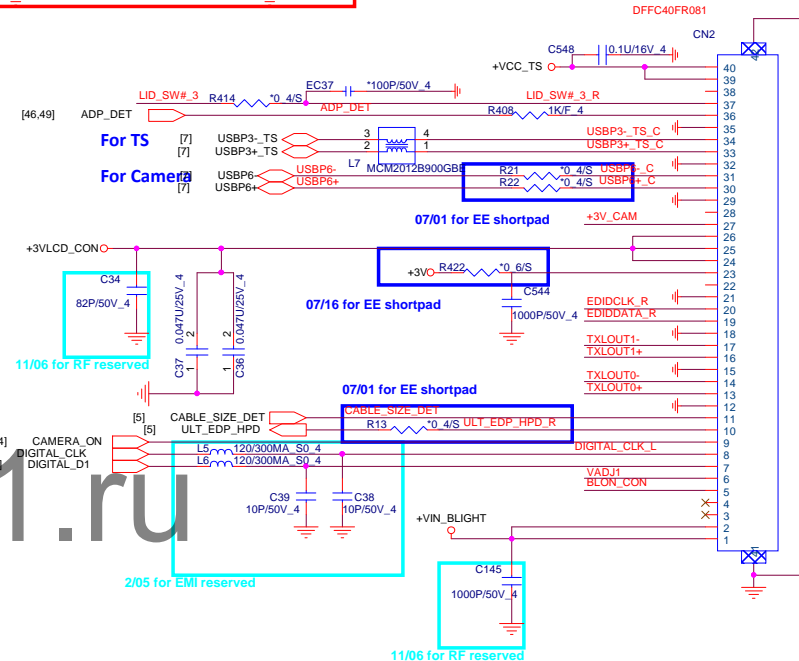
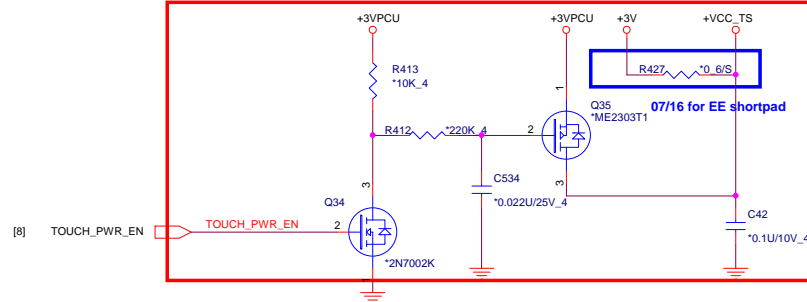
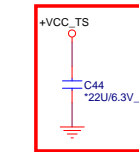


## 07/01 for EE shortpad



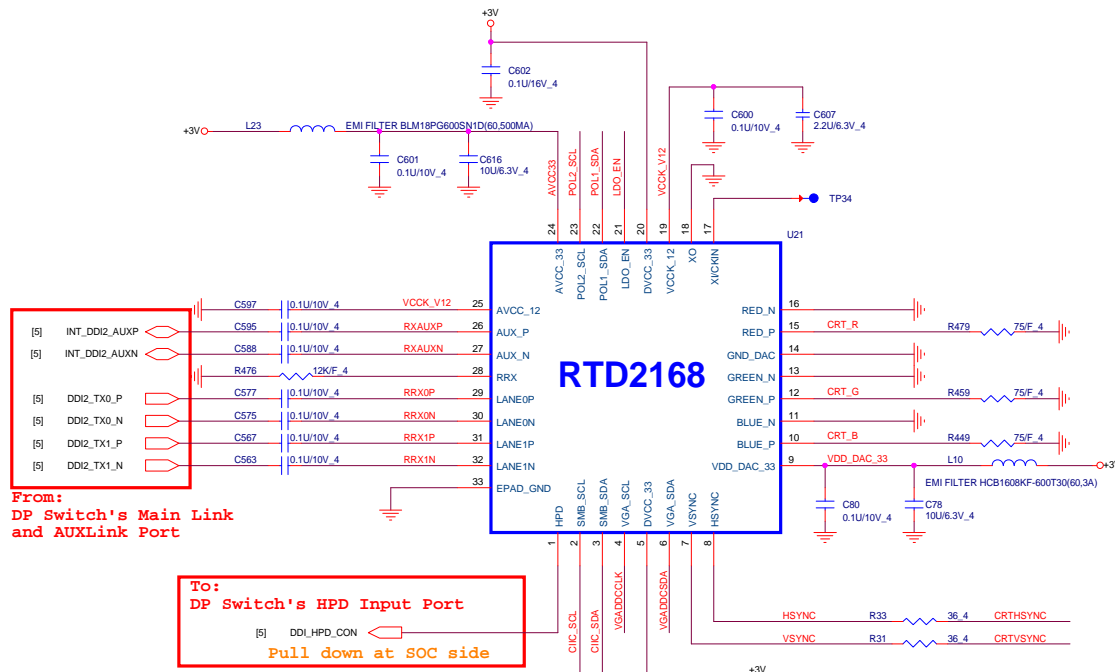
## LVDS Conn.

26

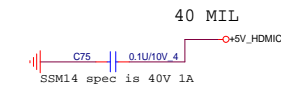
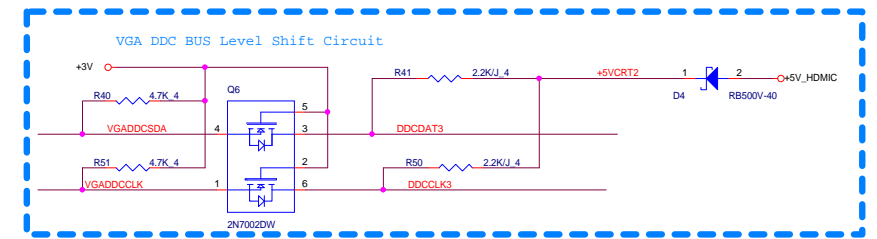
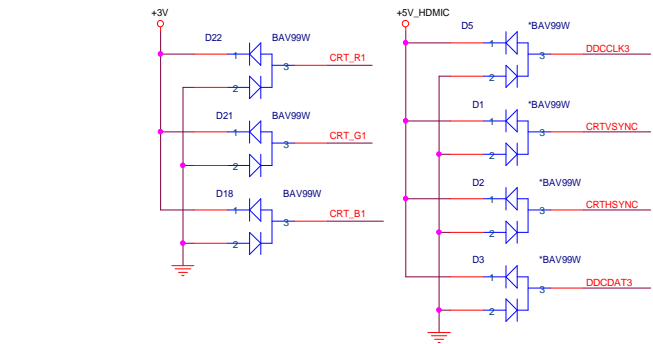


PROJECT:400 Series  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	26 - LCD CONN/LID/CAM/D-MIC	1A
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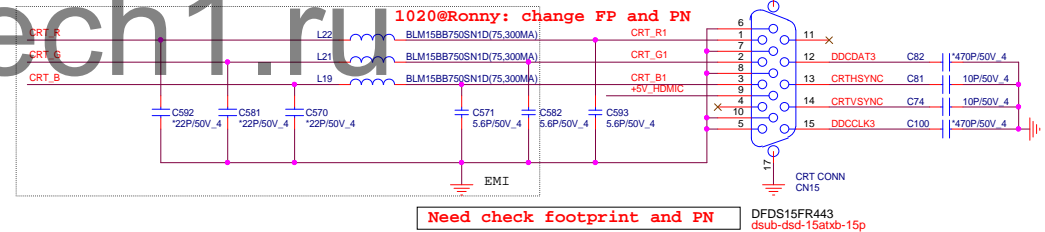


- Note:
- 1- C1,C3,C6,C8,C9,C11,C12,C19,C20 Should be close to chip
  - 2- C12 should be X5R material
  - 3- R1 should be 12K ohm with +/-1%
  - 4- R8, R9, R10 should be 75 ohm with +/-1%



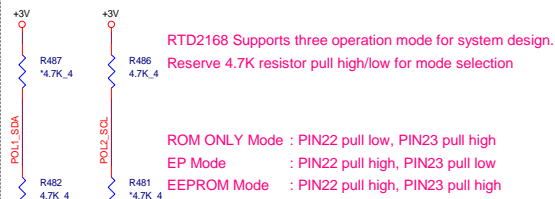
1103@RNY:  
need change L11~L13 to 0402 size PN and value

1020@Ronny: change FP and PN



### Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EPPROM MODE



### EEPROM MODE

In EEPROM mode, an additional EEPROM is needed.  
EEPROM should configure with following conditions.

- 1- EEPROM with a size of 16K-Byte
- 2- EEPROM device should be 2-byte addressing device
- 3- Slave address should configure as 0xA8

### CIIC\_SCL, CIIC\_SDA Connection

EP mode: Pin2, Pin3 connect to EC SMBUS  
ROM or EEPROM mode: connect to PCH SMBUS  
IIC Protocol is used

RTD2168 Slave Address:  
0x64/0x65 and 0x68/0x69

From PCH

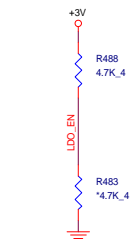


From EC



### Embedded LDO

Select VCCCK\_V12 source from external 1.2V or embedded LDO

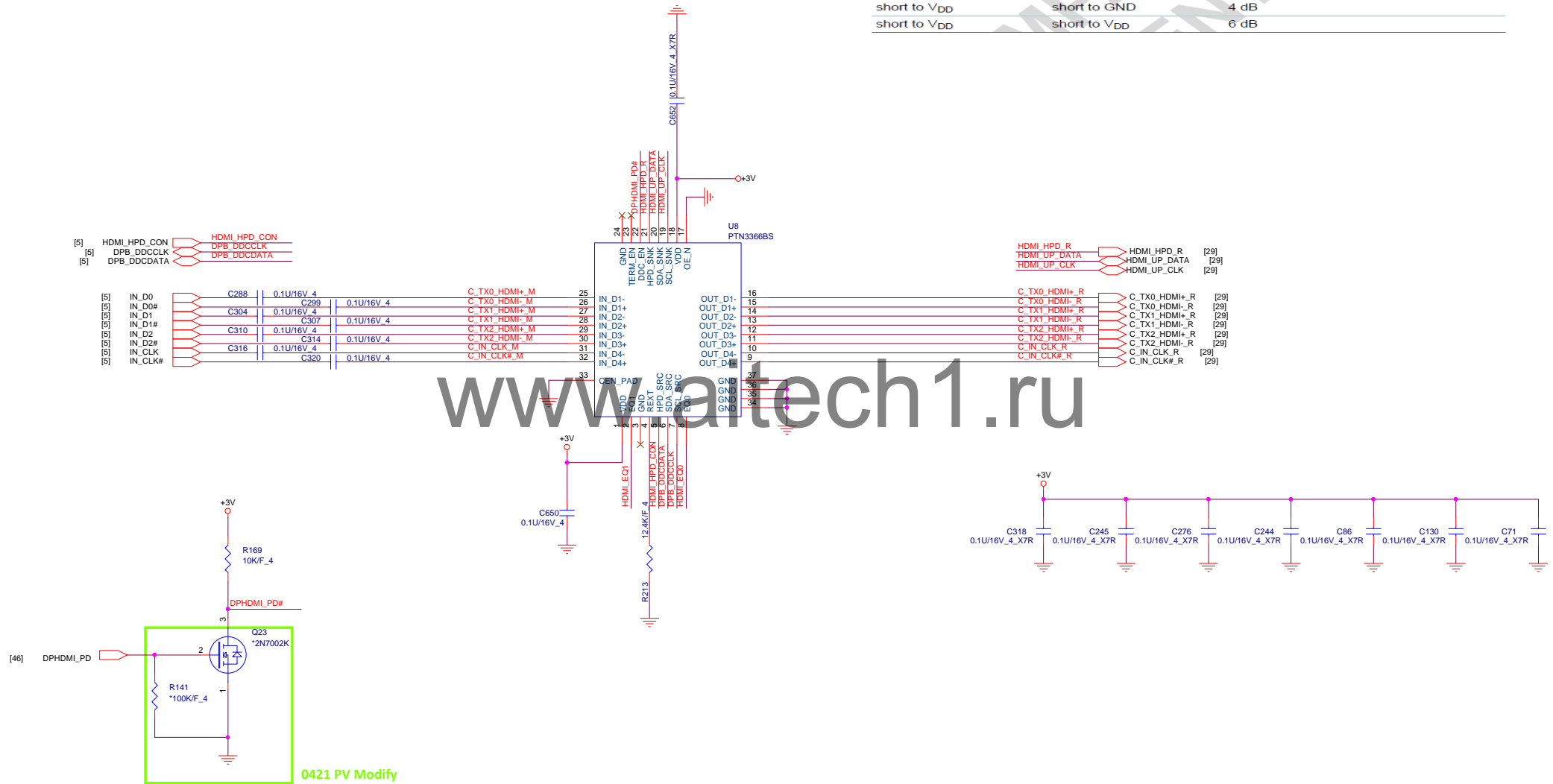


LDO_EN(PIN21)	
0	1
VCCCK_V12 from External 1.2V	VCCCK_V12 from Embedded LDO



**PROJECT : S Class-AMD**  
**Quanta Computer Inc.**

Size Custom Document Number DP to VGA  
Date: Monday, November 30, 2015 Sheet 27 of 65



Inputs		Equalization for 3 Gbit/s
EQ1	EQ0	
short to GND	short to GND	0 dB
short to GND	short to V <sub>DD</sub>	2 dB
short to V <sub>DD</sub>	short to GND	4 dB
short to V <sub>DD</sub>	short to V <sub>DD</sub>	6 dB

OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode



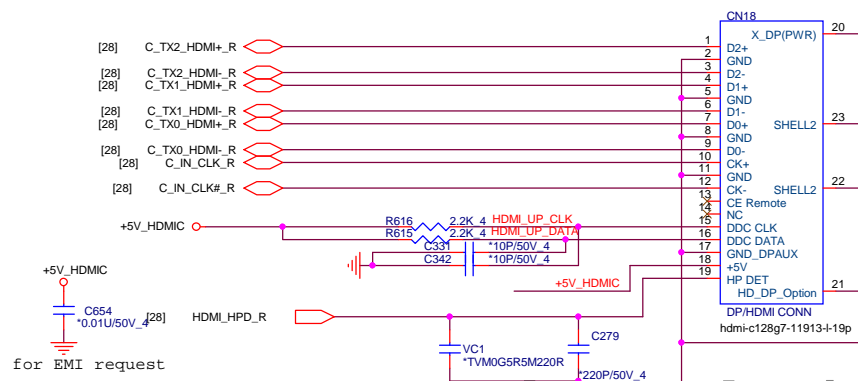
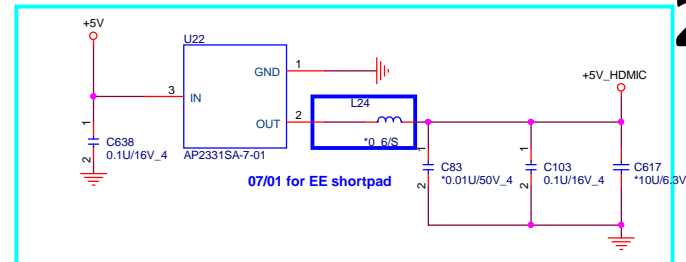
### EMI Solution

C_TX2_HDMI+_R	R208	150/F 4	C_TX2_HDMI-_R
C_TX1_HDMI+_R	R194	150/F 4	C_TX1_HDMI-_R
C_TX0_HDMI+_R	R178	150/F 4	C_TX0_HDMI-_R
C_IN_CLK#_R	R221	150/F 4	C_IN_CLK#_R

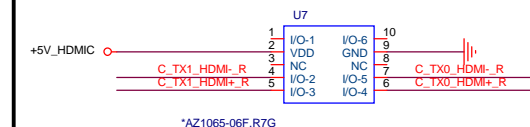
### HDMI SMBus Isolation

[28]	HDMI_UP_CLK	HDMI_UP_CLK
[28]	HDMI_UP_DATA	HDMI_UP_DATA

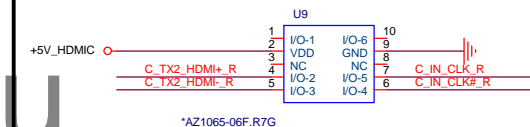
11/06 for change new SW



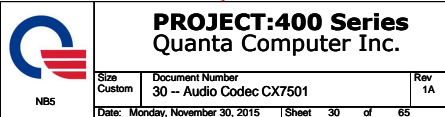
### ESD chip, reserve



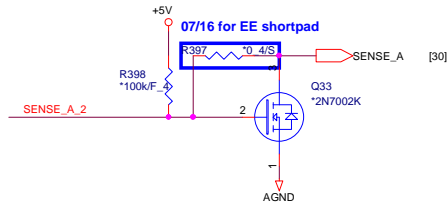
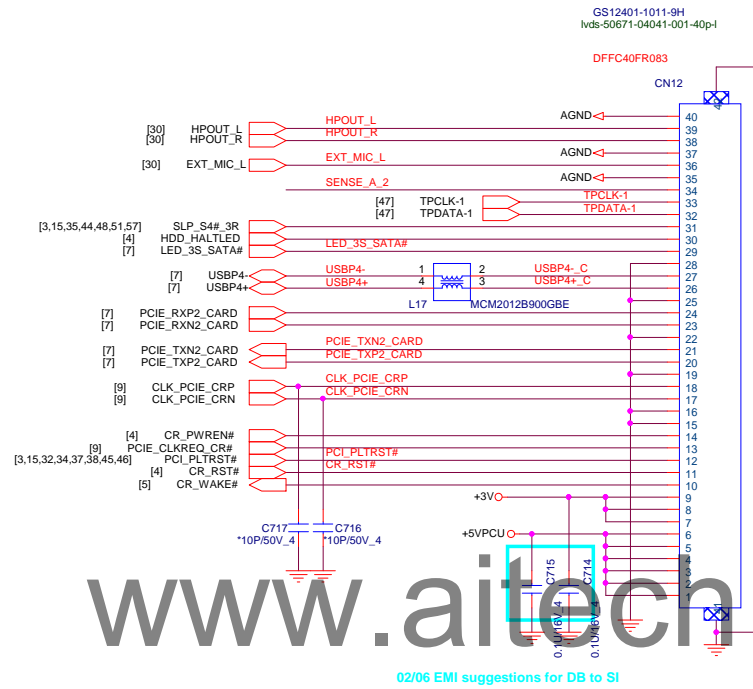
### ESD chip, reserve




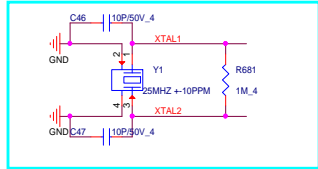
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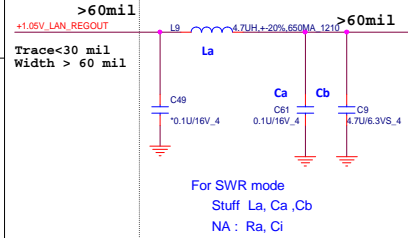
# USB/Card Reader/Headphone\_Mic Combo Jack Daughter Board Connector



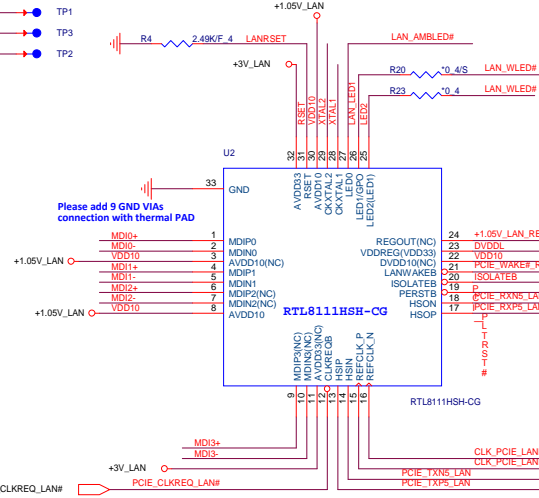
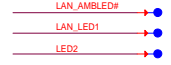
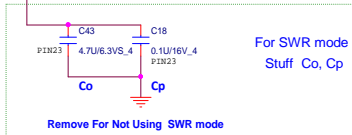
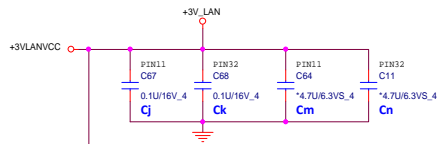
 NB5	<b>PROJECT:400 Series</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number 31 -- DAUGHTER BOARD CONN.	Rev 1A
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Power trace Layout 宽度&gt;60mil

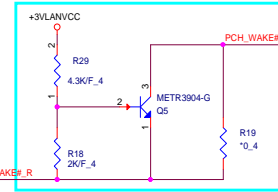


- \* Place Cj and Ck, close to each VDD33 pin-- 11, 32
- \* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)

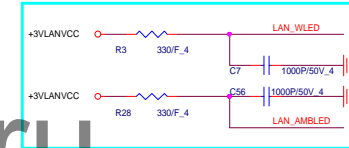


if ISOLATEB pin  
pull-low, the LAN  
chip will not drive  
it's PCI-E outputs  
(excluding  
PCI-E\_WAKE# pin)

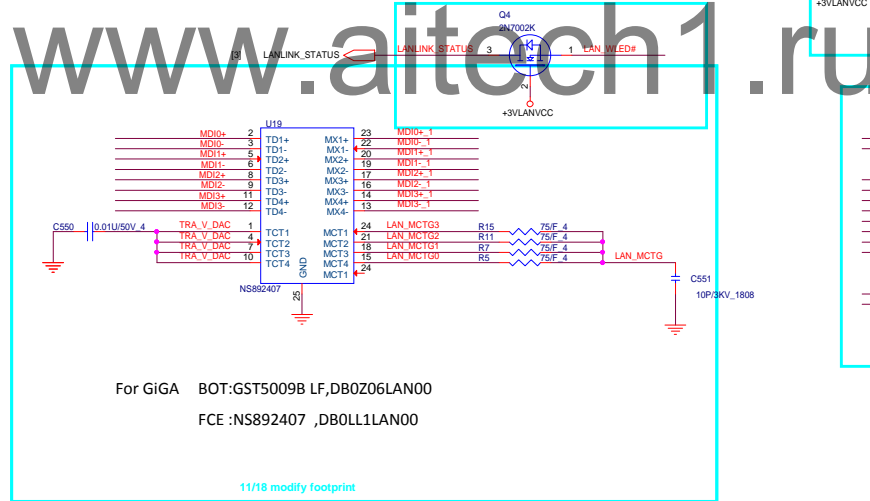
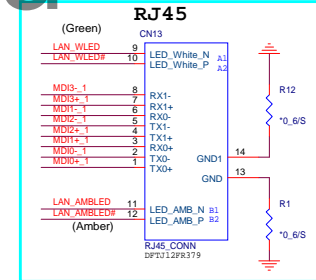
04/23 for SI to PV



04/23 for SI to PV



04/23 for SI to PV



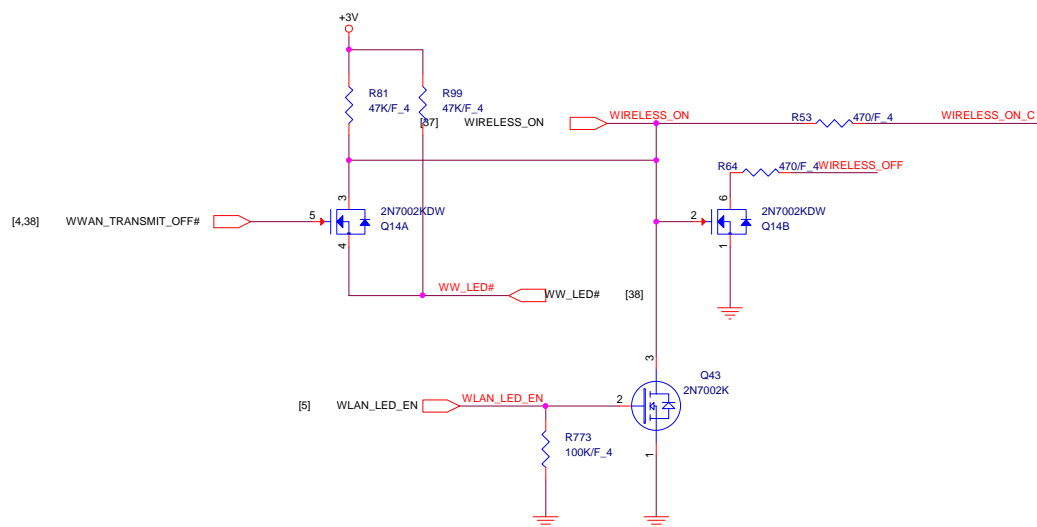
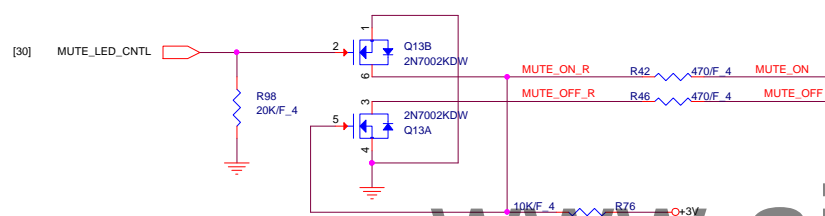
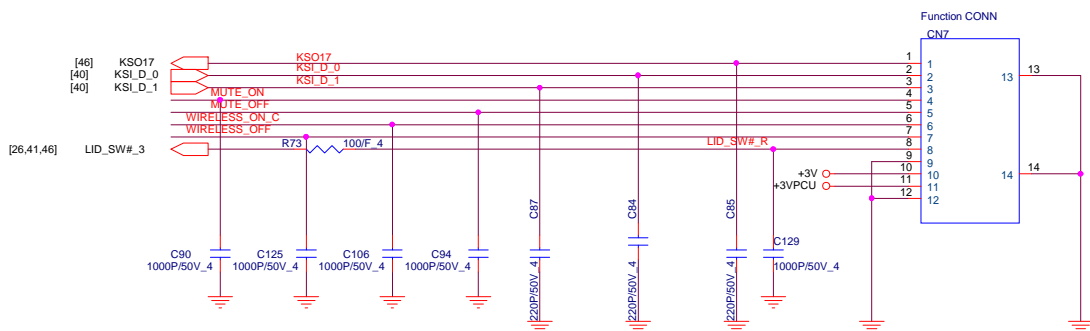
[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,33,34,36,38,42,44,45,49,55,57,63]

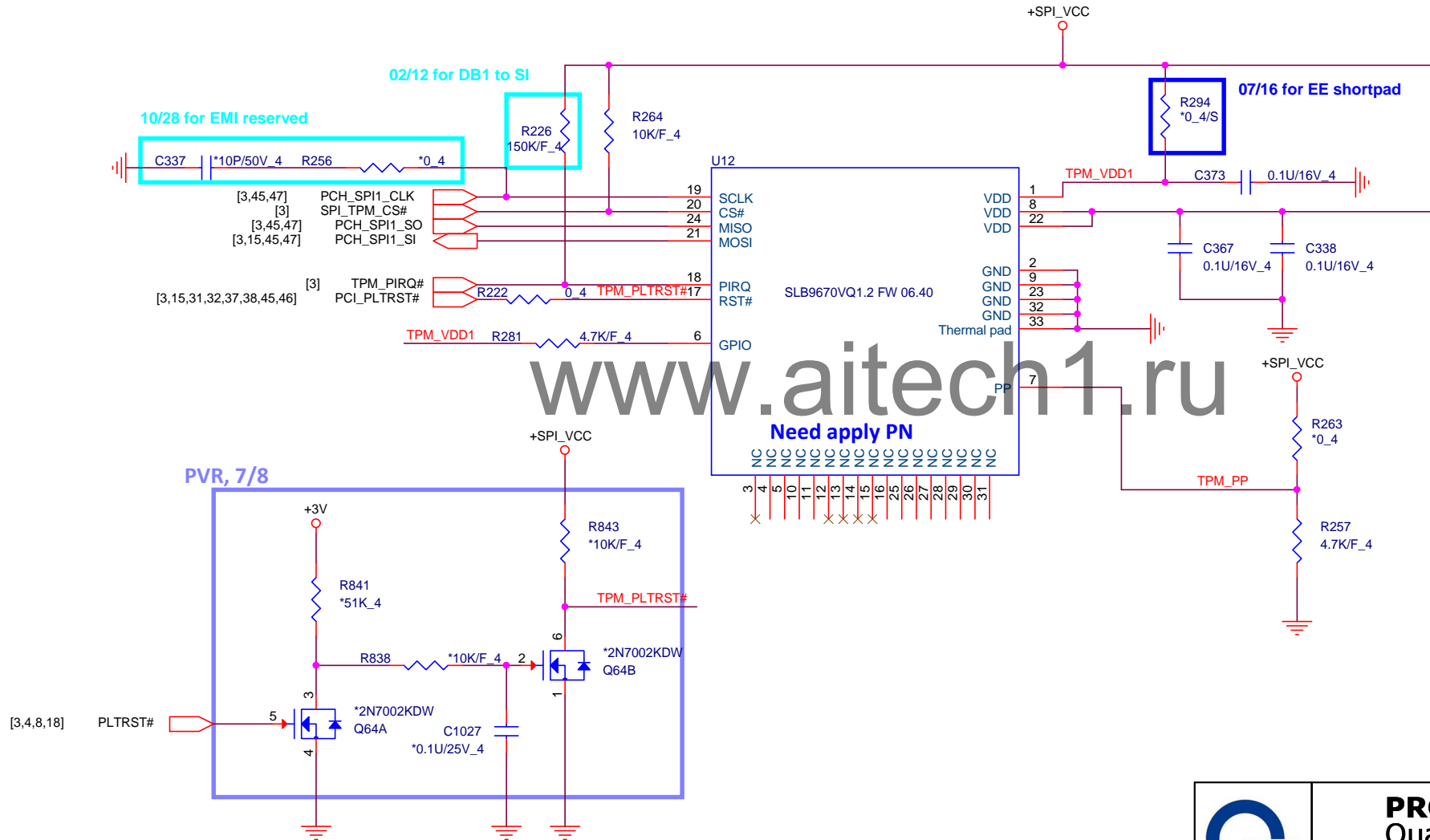
[57]

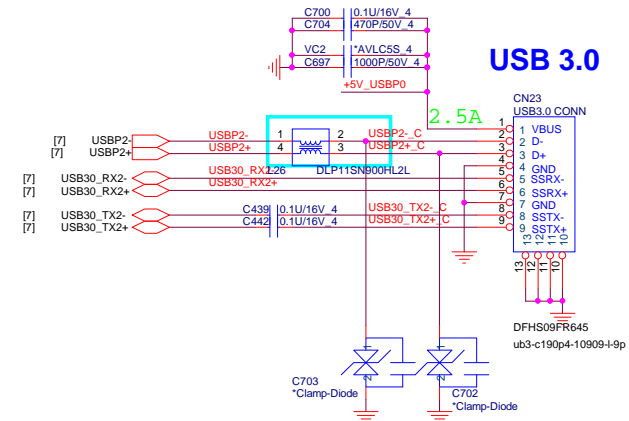
+3V  
+3V\_LANVCC

**PROJECT:400 Series**  
**Quanta Computer Inc.**

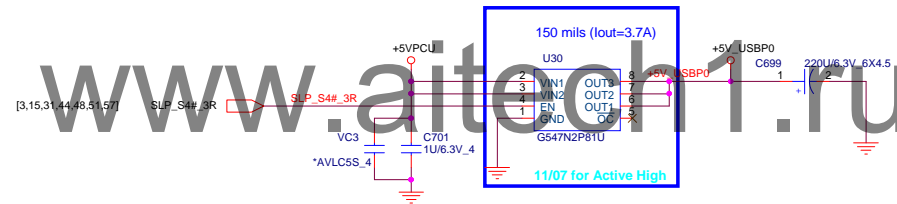
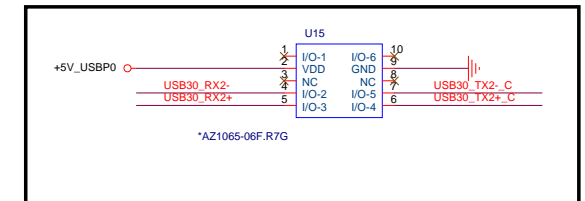
Size C Document Number  
**32 -- LAN RTL8111HSH-CG/RJ45**  
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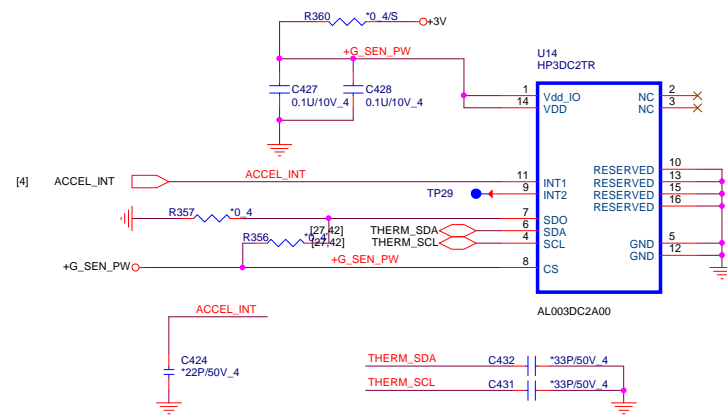




ESD chip, reserve



## Accelerometer Sensor



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[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,32,33,34,38,42,44,45,49,55,57,63]

+3V 

[3,10,15,26,33,37,38,40,41,42,44,45,46,48,49,50,51,53,54,57,60,62,63]

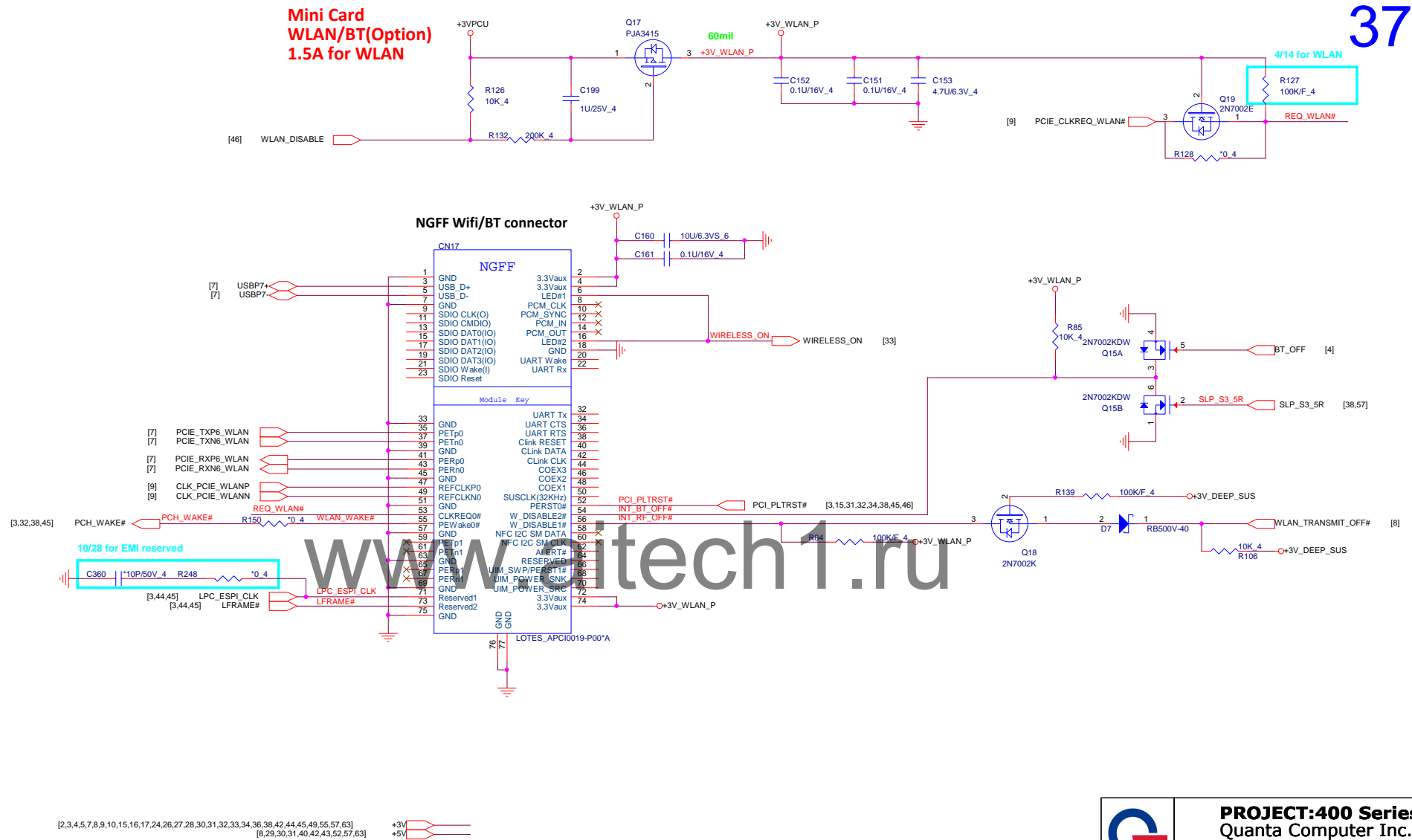
+3VPCU 

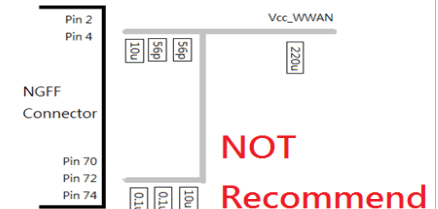
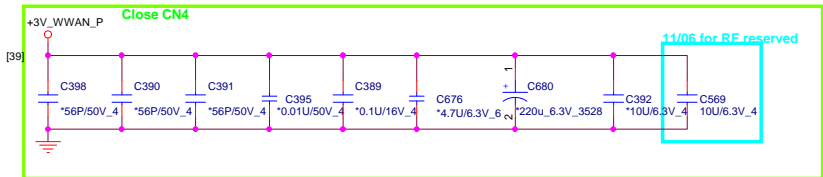


**PROJECT:400 Series**  
Quanta Computer Inc.

Size Custom	Document Number <b>36 -- TS and Accelerometer</b>	Rev 1A
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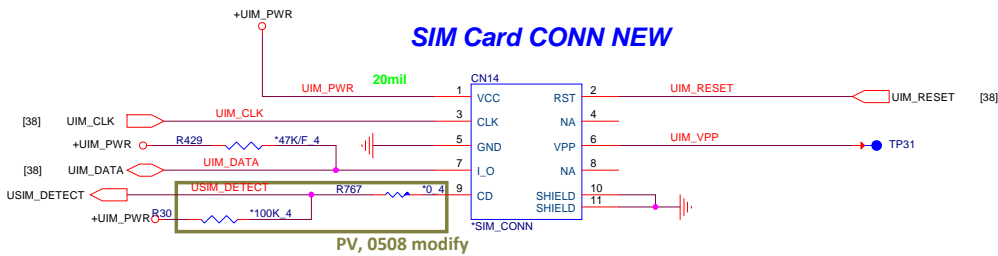


NOT  
Recommend

**WWAN(Optional)**  
Control of power must be allowed in all S0, S3, S4 and S5 states.

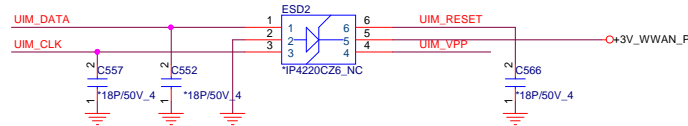
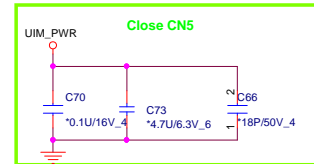
The schematic diagram illustrates the control circuit for the WWAN module. A +3V\_WWAN\_P supply is connected to a 10K\_4 resistor, which is connected to the non-inverting input (pin 2) of an inverter D13 (1SS355). The inverter's output (pin 1) is connected to the WWAN\_TRANSMIT\_OFF# pin of the PVR, 0714 module. The module's SLP\_S3\_5R pin is connected to the SLP pin of the Q27 (2N7002K) MOSFET. The MOSFET's source is connected to GND and its gate is connected to the WWAN\_TRANSMIT\_OFF# pin.

## SIM Card CONN NEW



Layout Note:

1. UIM\_RESET, UIM\_CLK, UIM\_DATA routing as short as possible  
Route into ESD then go out
2. Avoid routing the SIM\_CLK and SIM\_DATA lines in parallel over distances  $\geq 2$  cm
3. Position the SIM connector from the WWAN module  $\leq 100$ mm if possible, NOT exceed length is 150mm.

Trace Length and Routing<sup>u</sup>

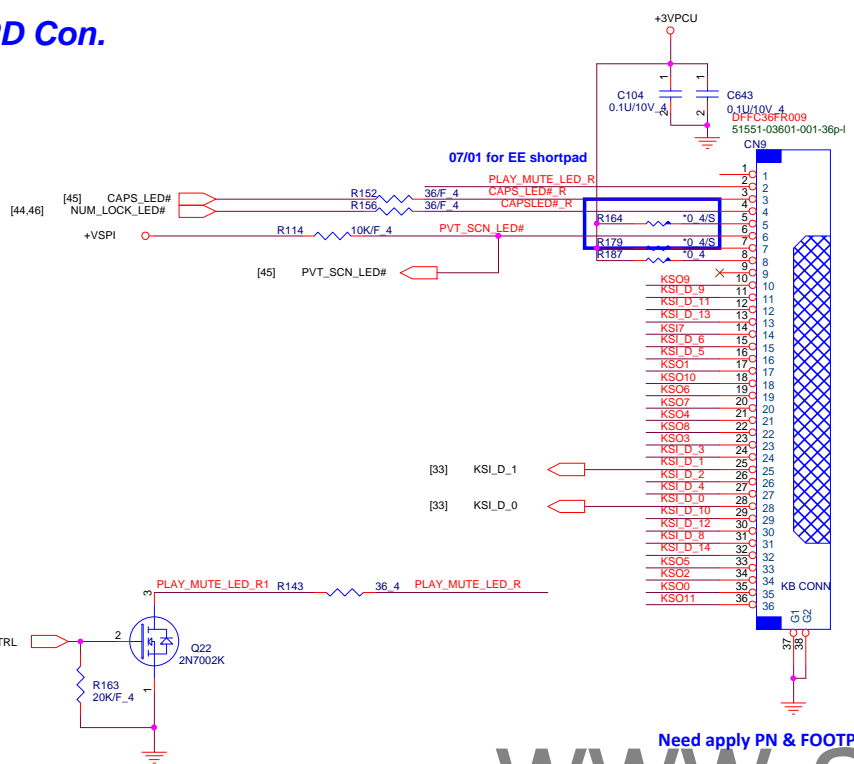
- Special attention should be paid to SIM traces (UIM\_CLK, UIM\_DATA and UIM\_RST) to minimize the trace lengths between the SIM slot and the WAN NGFF slot. **Minimizing the signal lengths and traces will reduce possibility of SIM signal integrity issues.** Recommended maximum length is 100mm. Not to exceed length is 150mm.<sup>u</sup>
- Minimum distance between UIM\_CLK and UIM\_DATA should be 20 mils. Static signals such as UIM\_RST can be routed between UIM\_CLK and UIM\_DATA to conserve space if needed.<sup>u</sup>
- It is recommended that SIM traces be isolated from other high-speed switching signals, as noise can couple into the SIM signals. Keep a minimum distance of 20 mils between UIM\_CLK, UIM\_DATA and any other high-speed switching signals.<sup>u</sup>
- Placing the SIM card on a daughter card is also not recommended as the interconnect may impact SIM signal integrity.<sup>u</sup>

SIM Power<sup>u</sup>

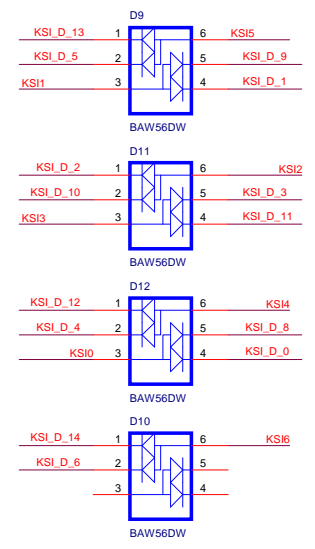
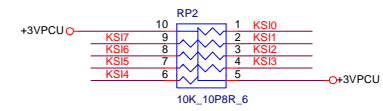
- The UIM\_PWR trace width must be at least 20 mils. Sub-planar routing is recommended.<sup>u</sup>
- Implement additional power filtering to SIM card power to ensure clean power is supplied to minimize any possible noise ripple effects. At a minimum, place a 0.1uF and a 4.7uF capacitor on the UIM\_PWR supply and locate near the SIM connector.<sup>u</sup>

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RF cap

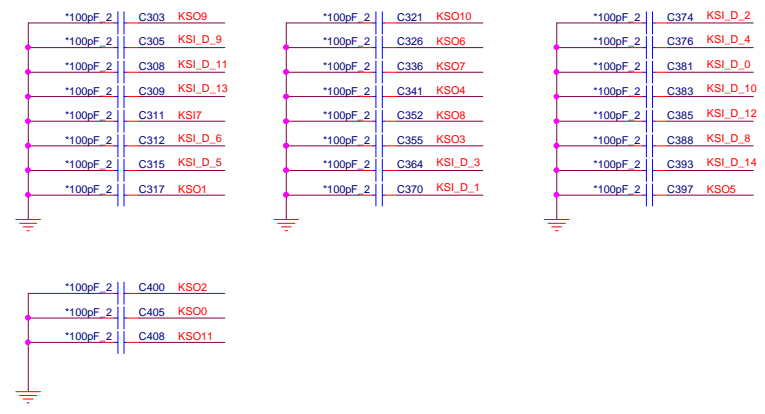
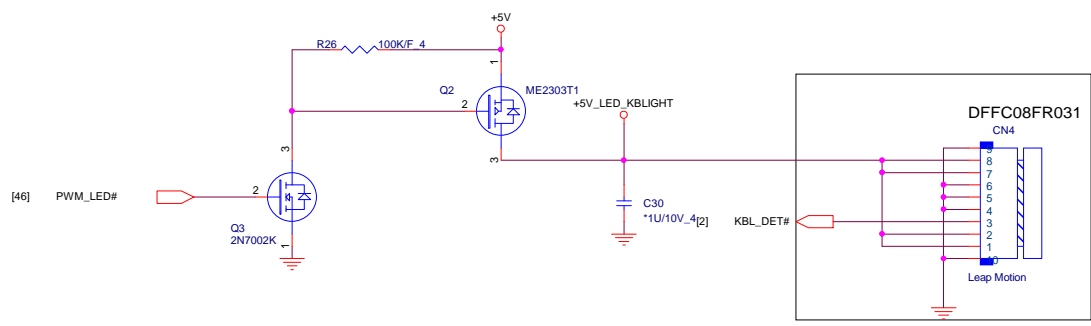


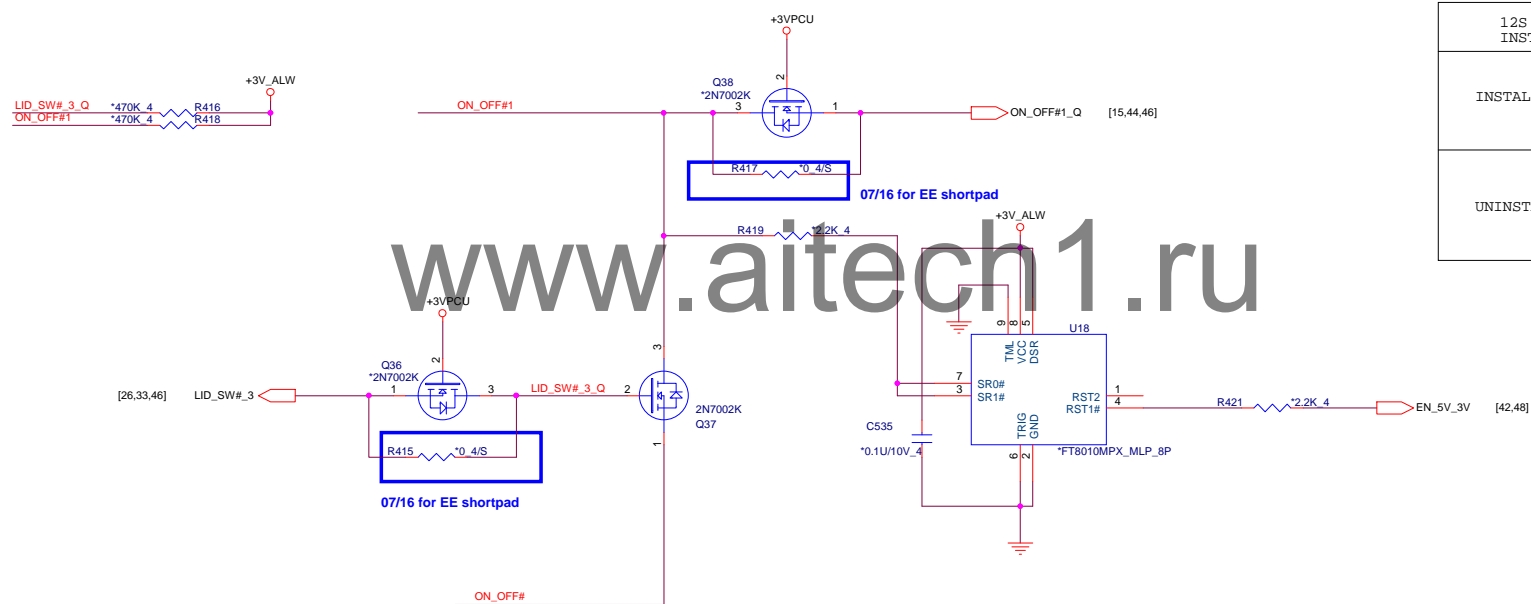
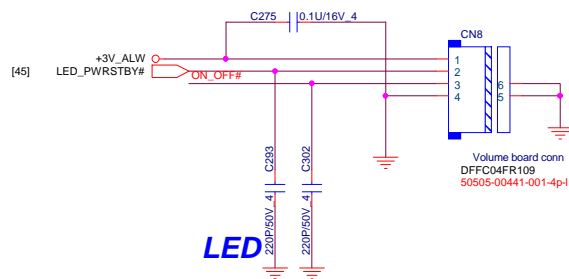
KEYBOARD PULL-UP



Need apply PN & FOOTPRINT

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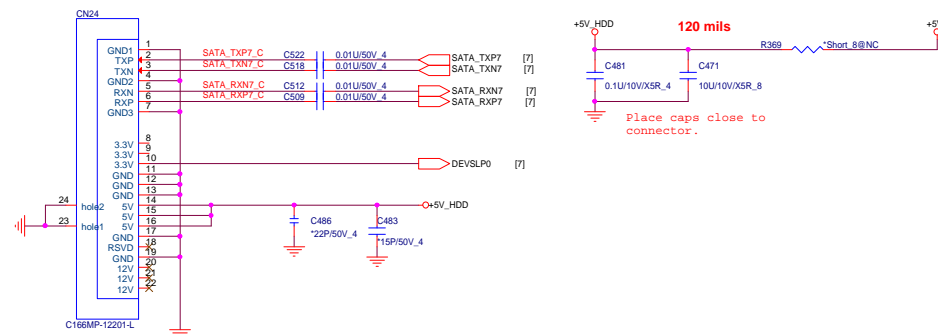


12S RESET MODE INSTAL FOR DB0		
INSTAL	R10702 R10704 R10701 U9068	R10703 R581 R595
UNINSTAL	R10754 Q7080	R10755 Q7081

[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,32,33,34,36,38,42,44,45,49,55,57,63] +3V  
[8,29,30,31,40,42,43,52,57,63] +5V  
[9,45,48,49,50,57,62,63] +3V\_ALW



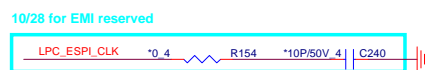
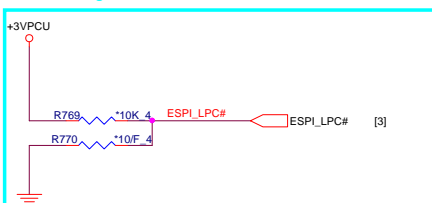
## SATA-HDD



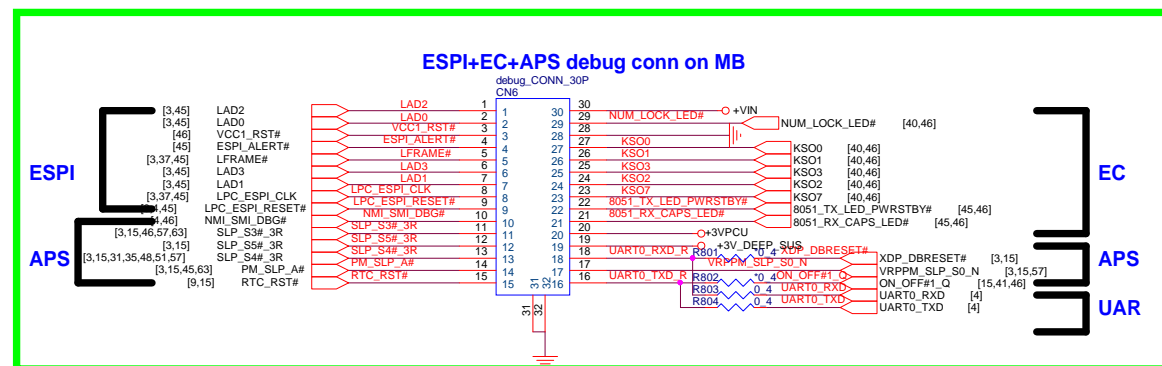
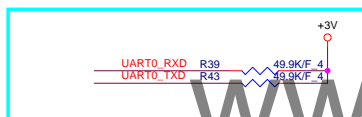
EMI cap

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02/10 for Bellagio ESPI



11/04 for check list



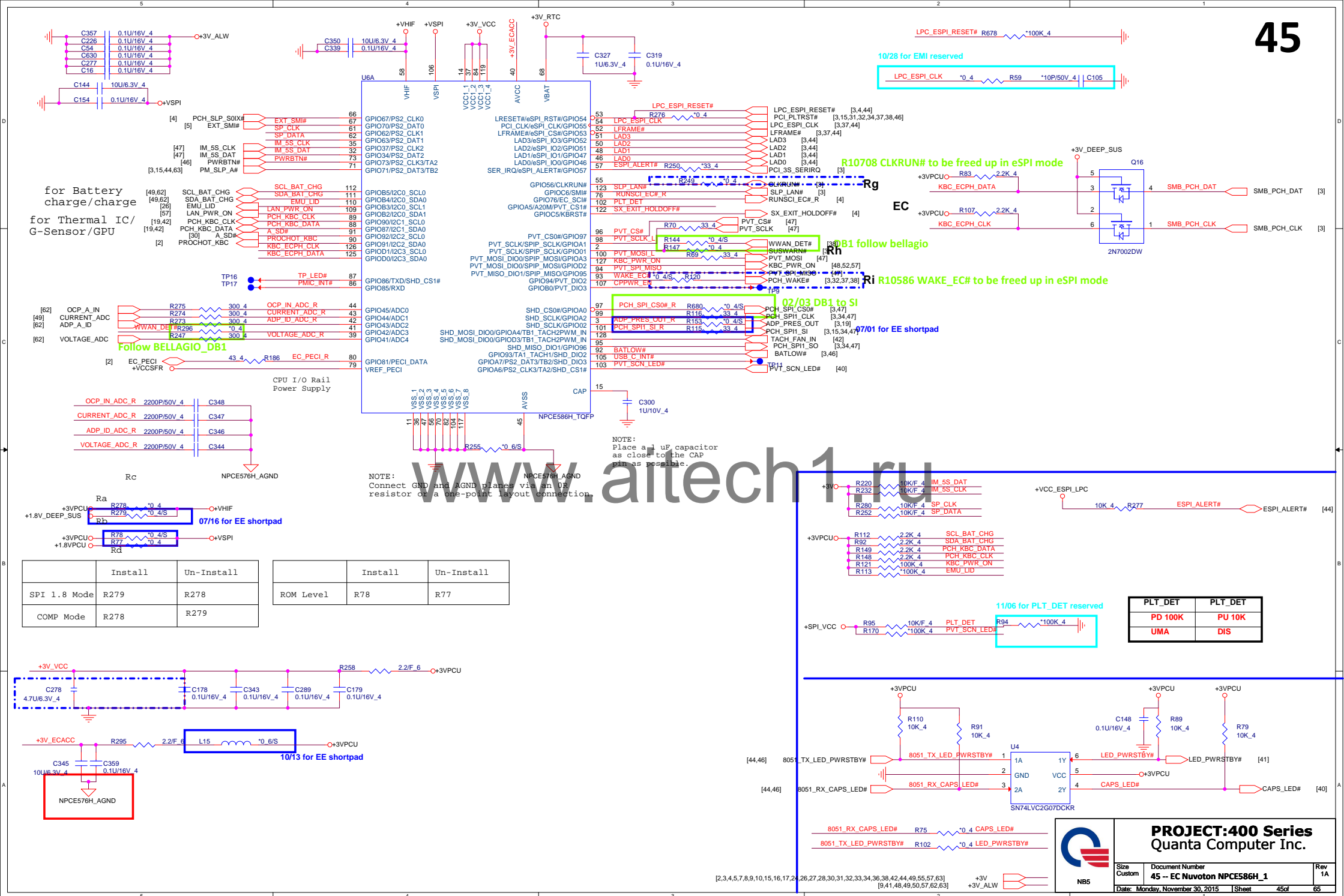
LPC &amp; ESPI TABLE

	LPC MODE	ESPI MODE
R771	INSTAL	UNINSTAL
R769	UNINSTAL	INSTAL
R770	INSTAL	UNINSTAL

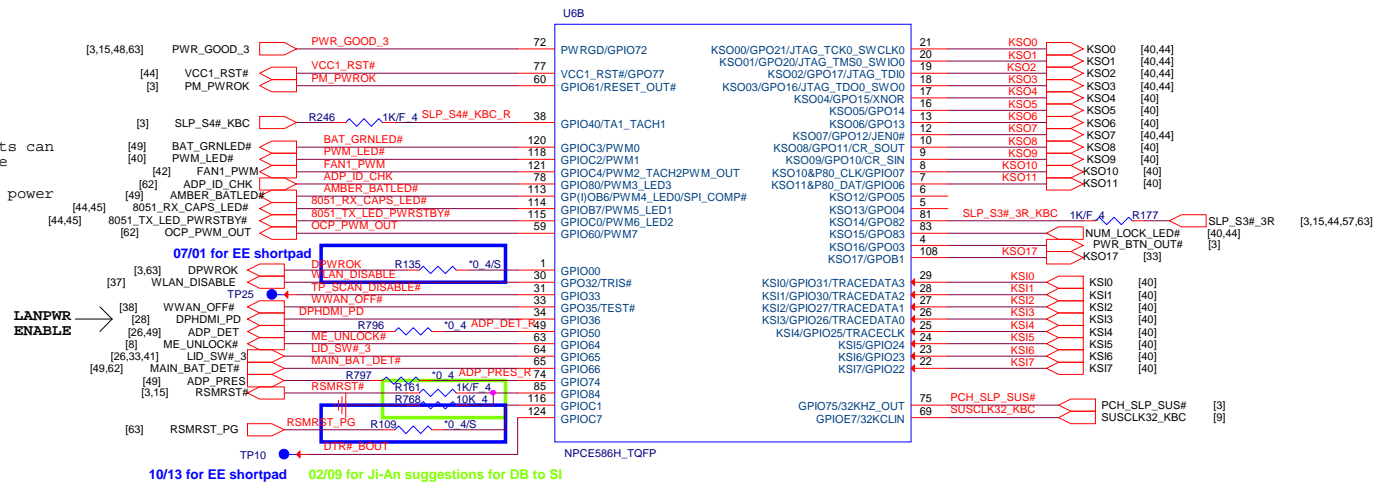
LPC &amp; ESPI TABLE

	LPC MODE	ESPI MODE
R658 <b>Ra</b>	INSTAL	UNINSTAL
R646 <b>Rb</b>	INSTAL	UNINSTAL
R659 <b>Rc</b>	INSTAL	UNINSTAL
R656 <b>Rd</b>	INSTAL	UNINSTAL
R649 <b>Re</b>	INSTAL	UNINSTAL
R657 <b>Rf</b>	INSTAL	UNINSTAL
R249 <b>Rg</b>	INSTAL	UNINSTAL
R147 <b>Rh</b>	INSTAL	UNINSTAL
R120 <b>Ri</b>	INSTAL	UNINSTAL
R276 <b>Rj</b>	INSTAL	UNINSTAL
R678 <b>Rk</b>	UNINSTAL	INSTAL

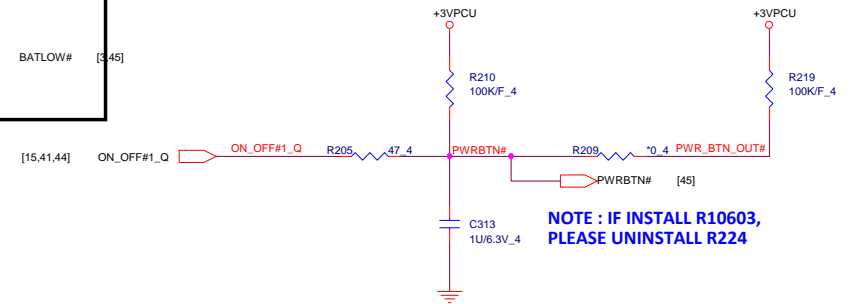
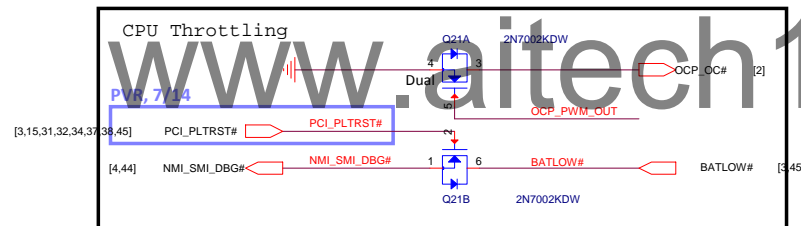




All the PWM outputs can directly drive the cathode of a LED connected to 3.3V power

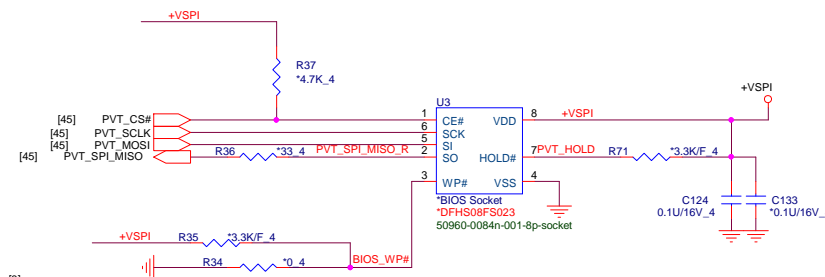


PV, 0415 add R798 connect ADP\_DET and ADP\_PRES\_R

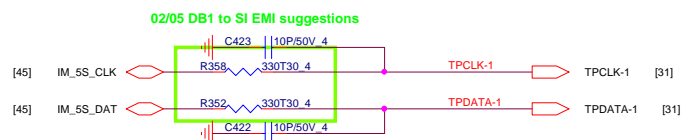


Vender	Size	P/N
Winbond	16MB	AKE38FP0N03
Socket		DFHS08FS023

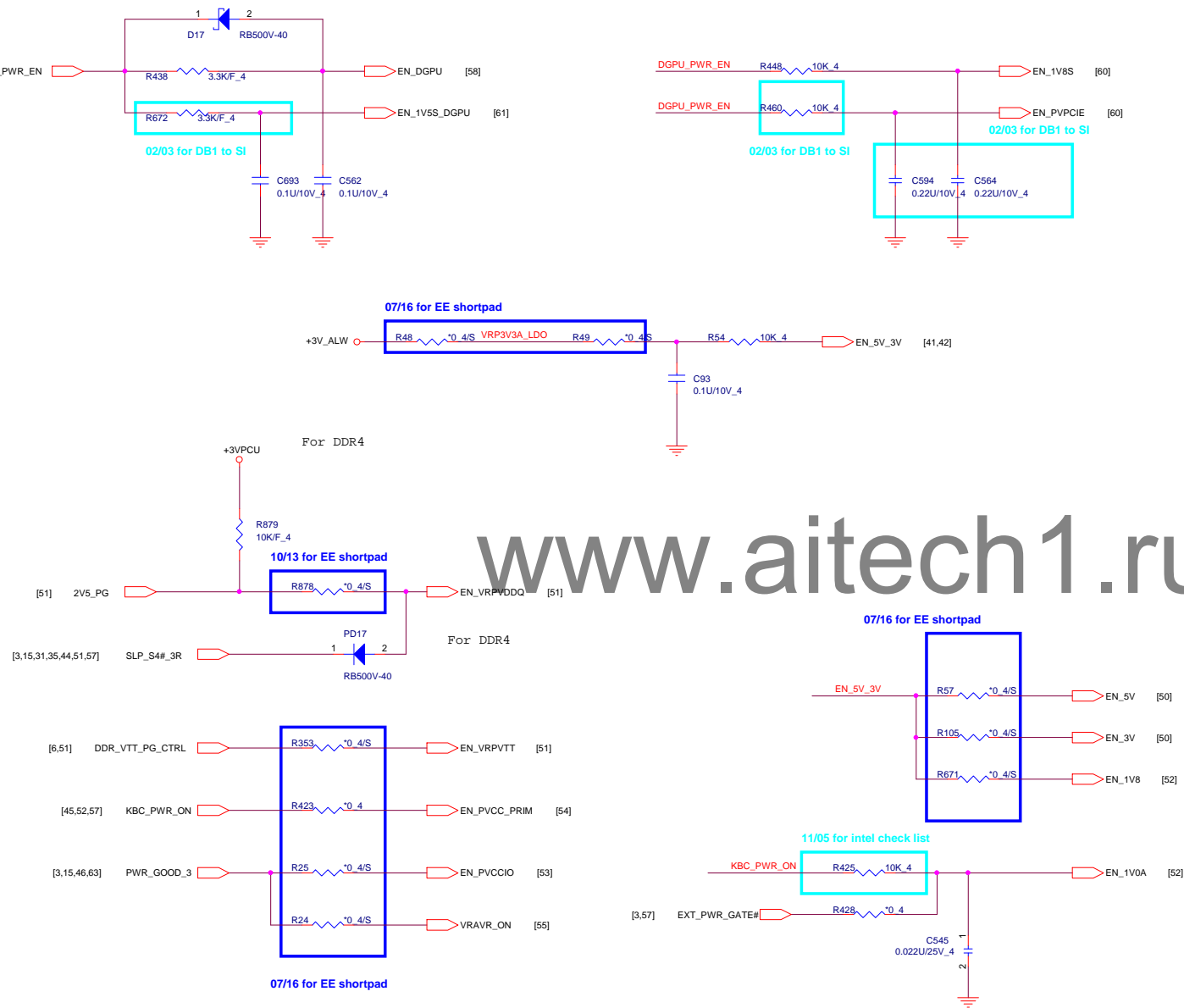
**PCH 6\*5mm WSON 16M  
SPI ROM Socket**

[illegible]

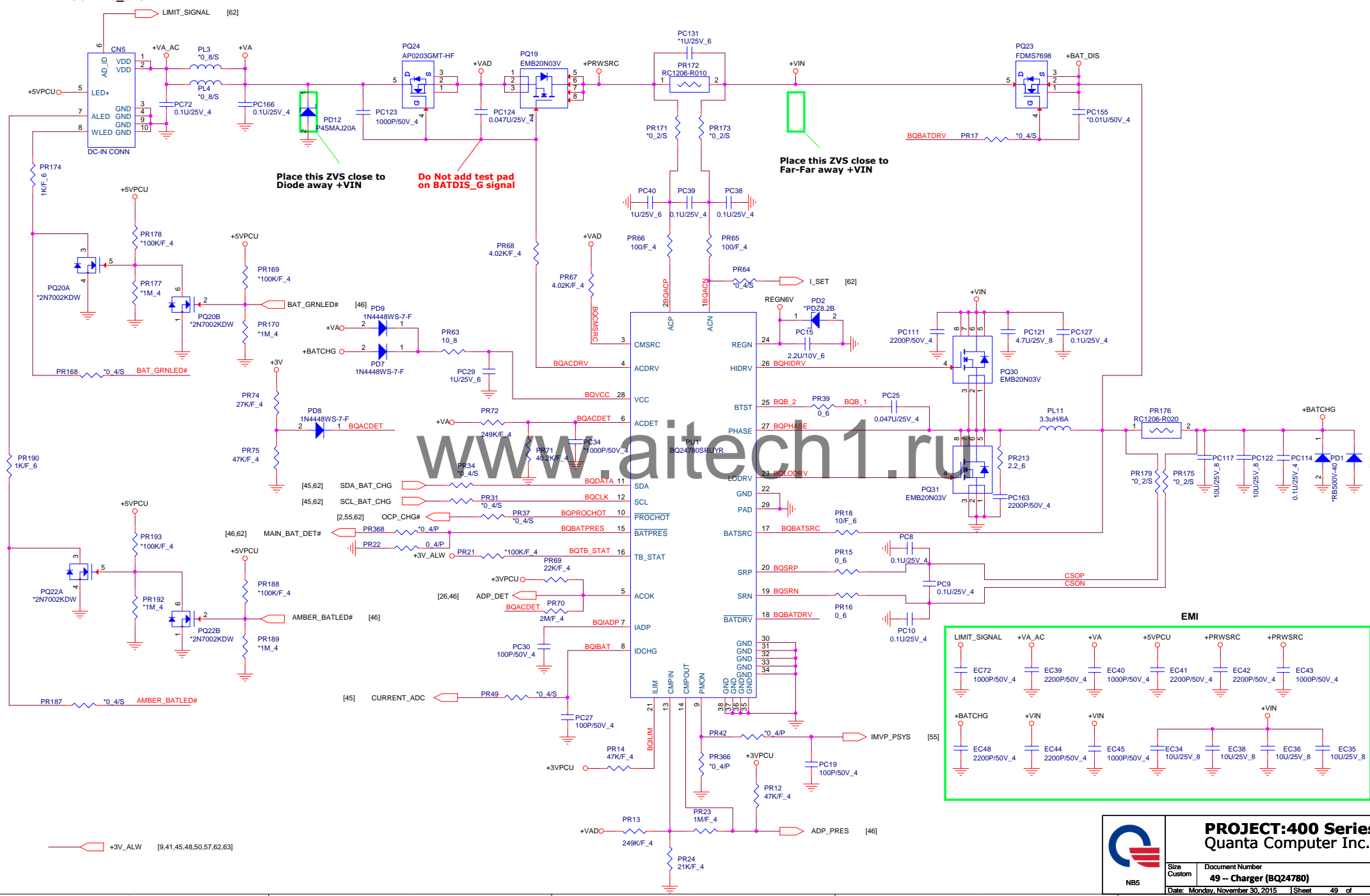
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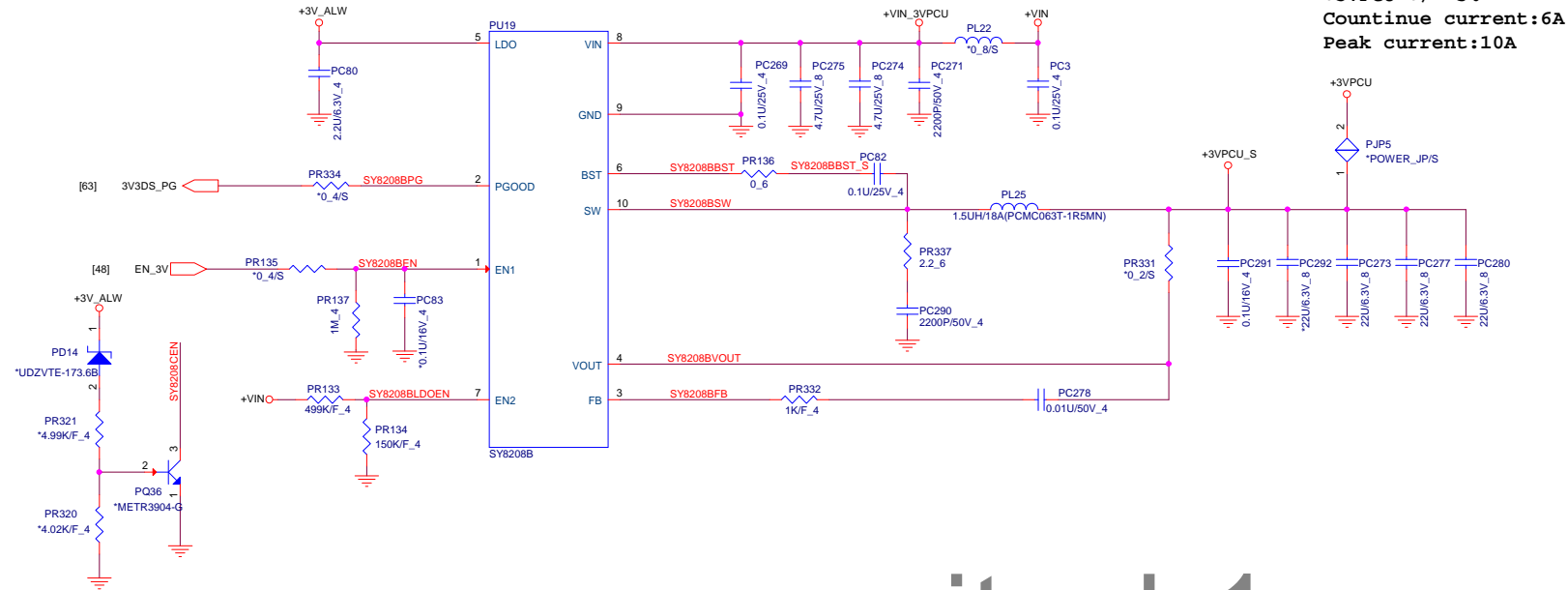
## POWER TO EE NET NAME CONNECTION



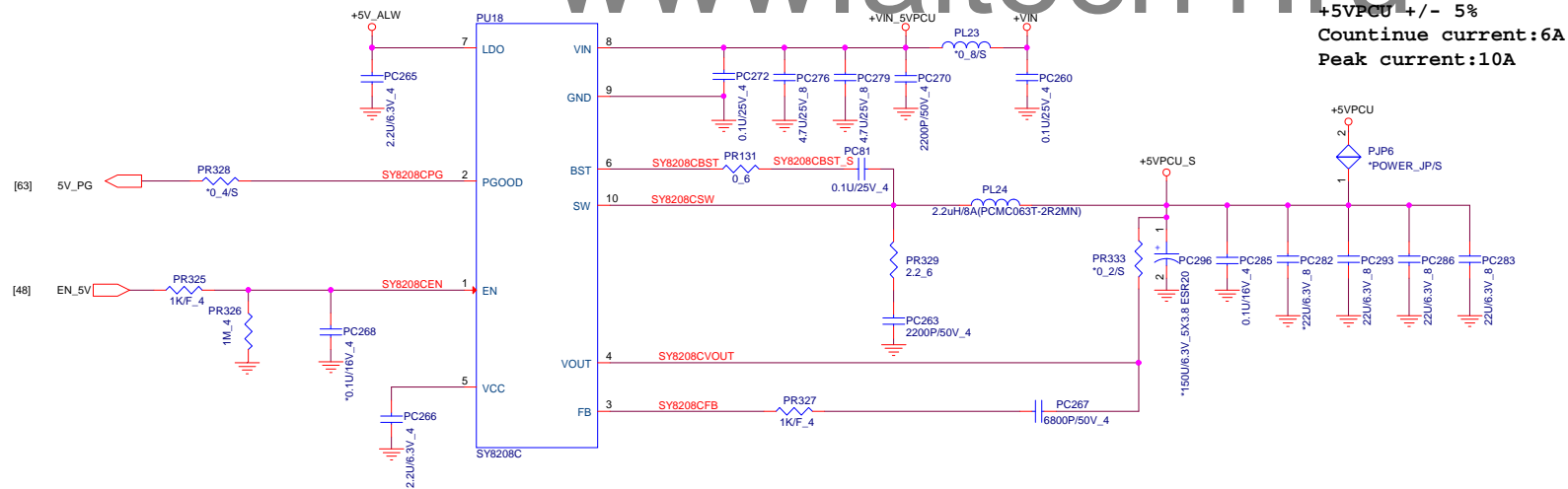
## 90W DC\_JACK



Do Not add test pad  
on +3VPCU

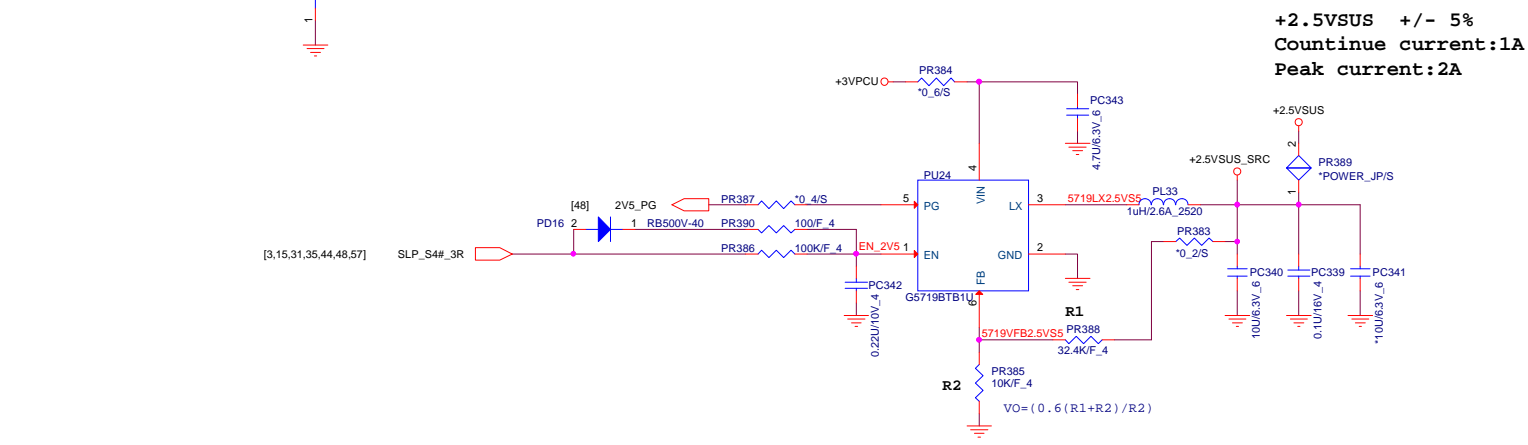
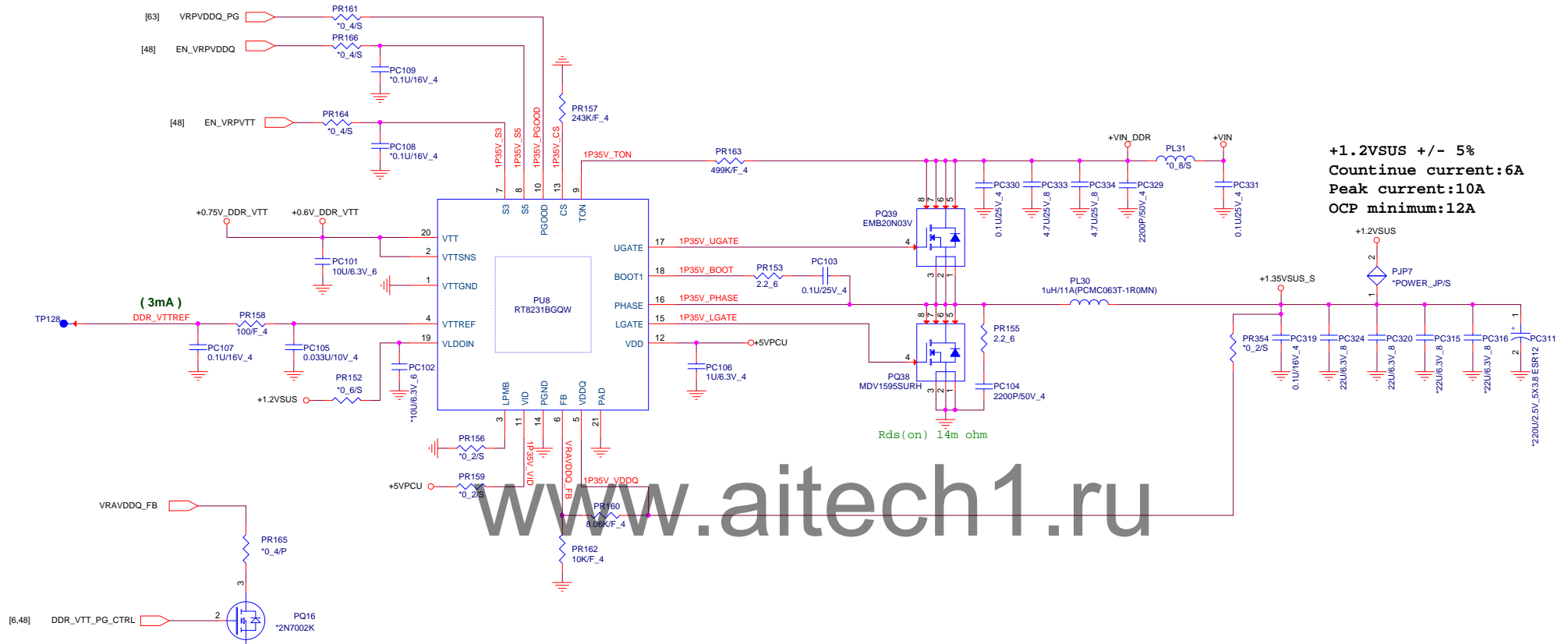


Do Not add test pad  
on +5VPCU

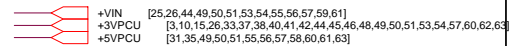
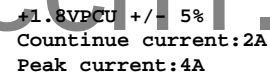


**PROJECT:400 Series**  
**Quanta Computer Inc.**

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	50 - 3/5VS5 (SY8208B/SY8208C)	1A
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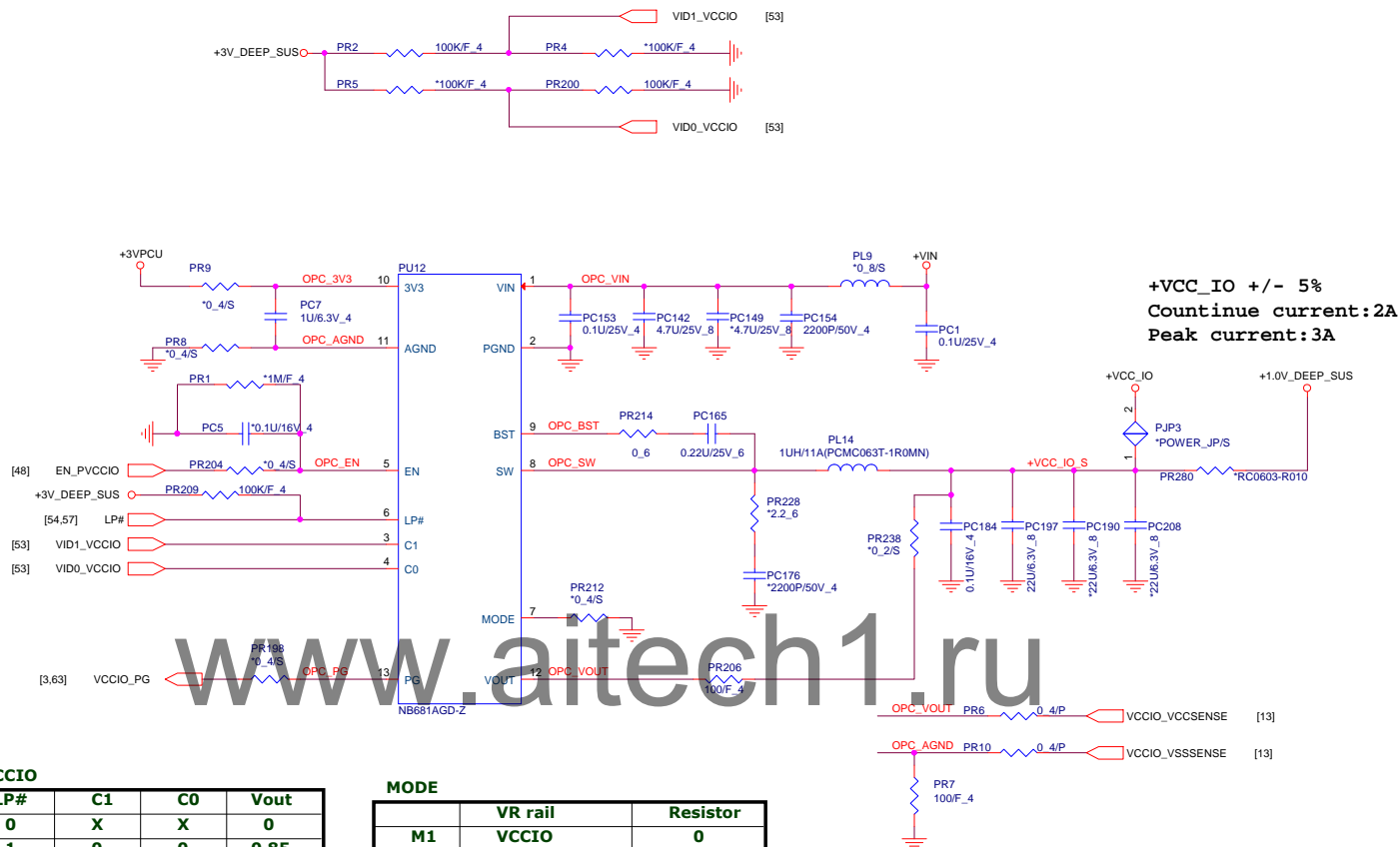
+1.2VSUS [6,13,16,17,57]  
+2.5VSUS [16,17]





[25,26,44,49,50,51,52,54,55,56,57,59,61]  
[9,41,45,48,49,50,57,62,63]  
[5,13,15]

+VIN  
+3V\_ALW  
+VCC\_IO

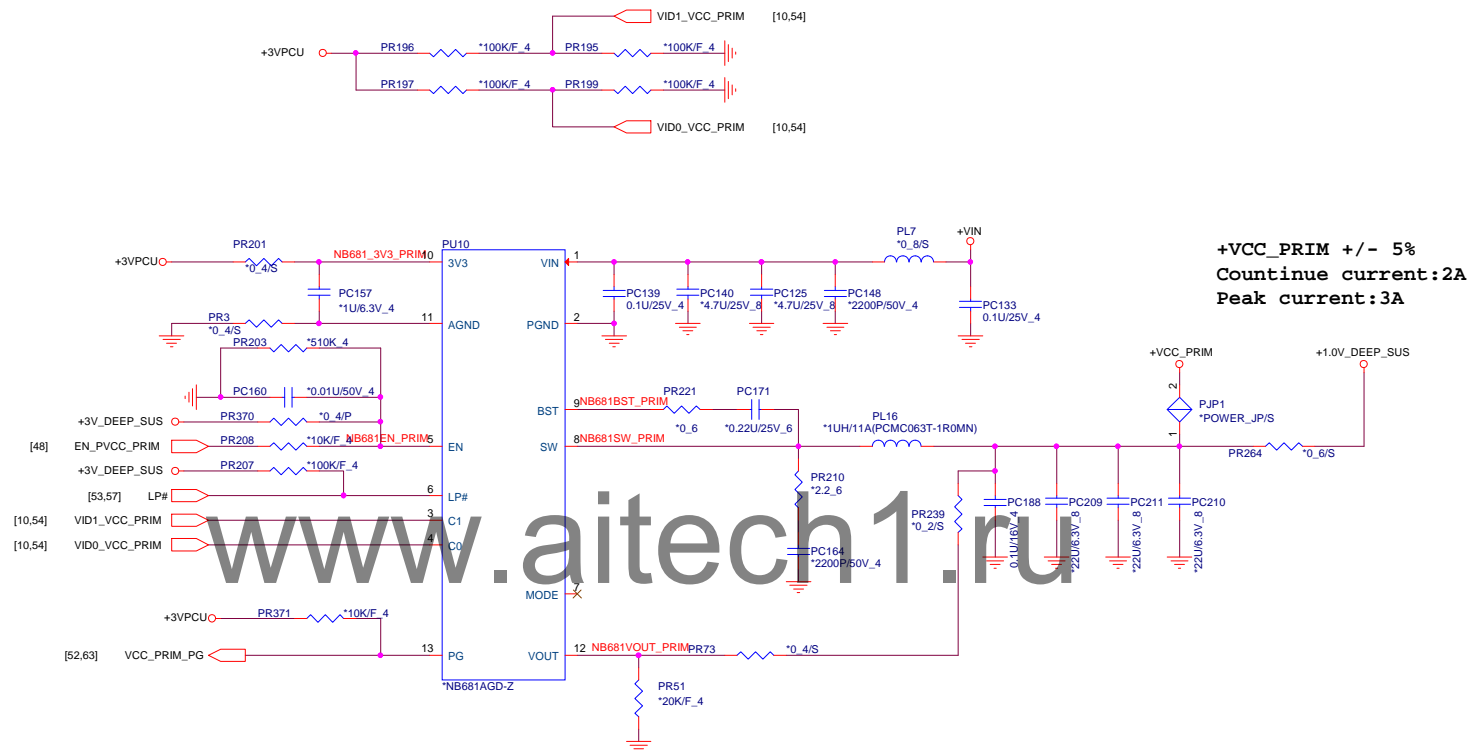


#### VCCIO

LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.85
1	0	1	0.875
1	1	0	0.95
1	1	1	0.975

#### MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

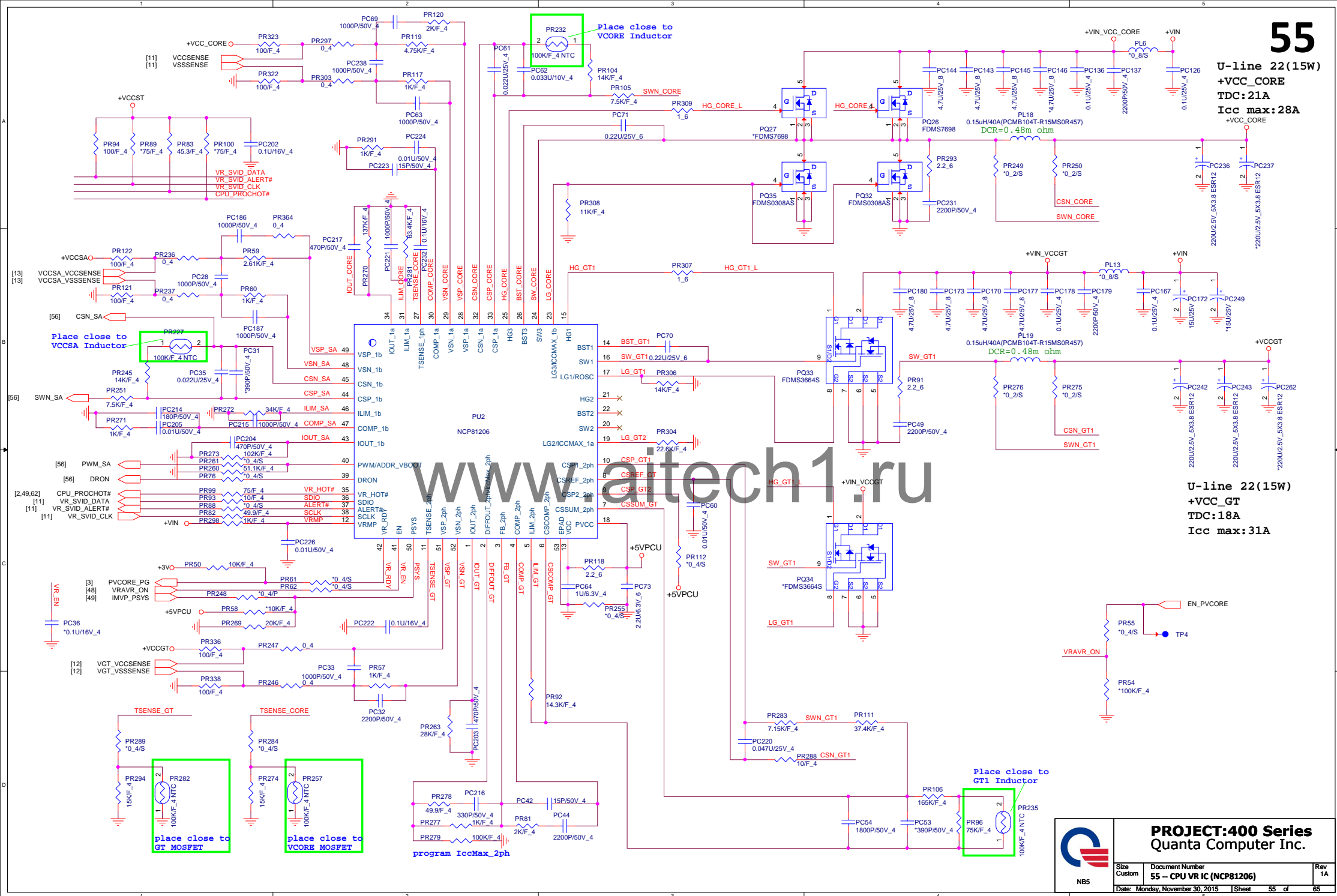


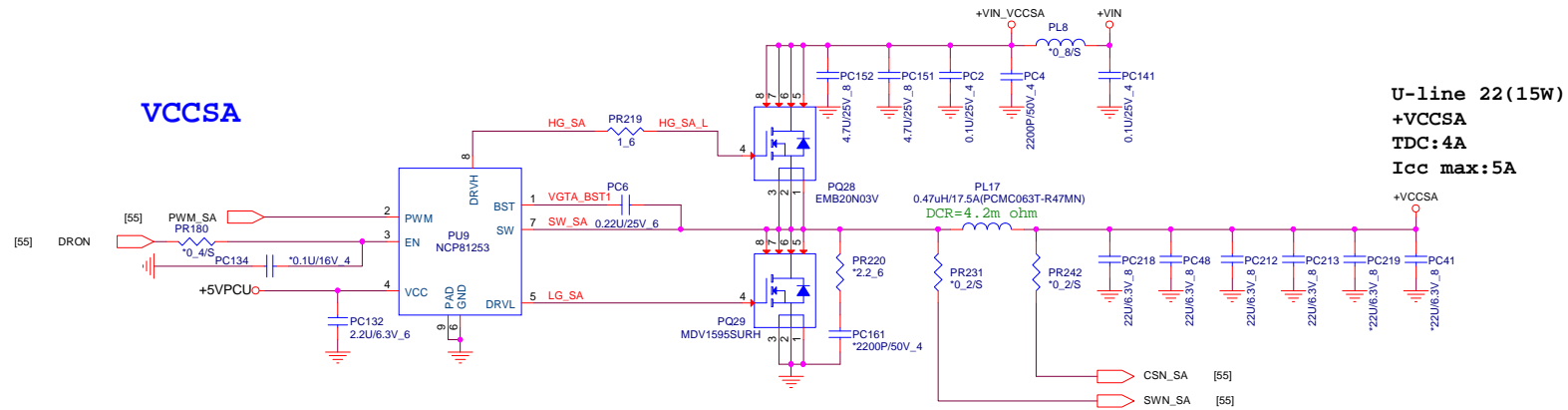
**VCC\_PRIM**

LP#	C1	C0	Vout
0	X	X	0.7
1	0	0	0.8
1	0	1	0.9
1	1	0	0.95
1	1	1	1.0

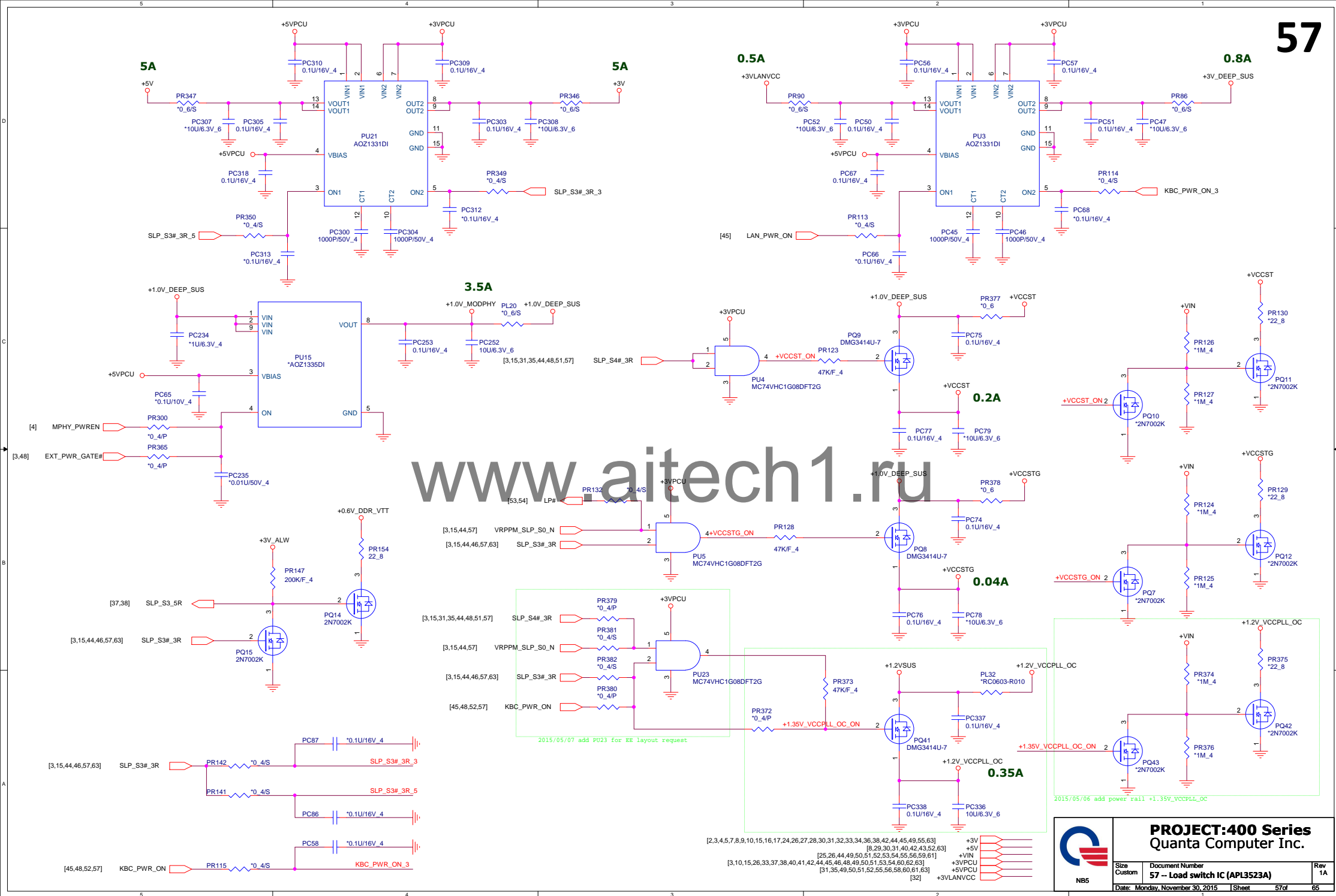
**MODE**

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

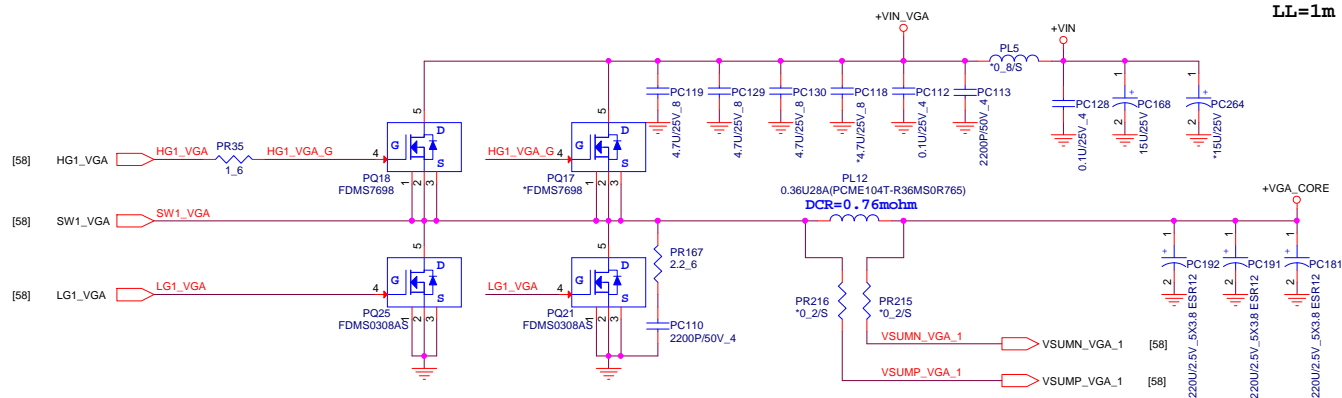




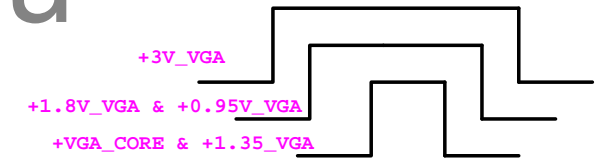
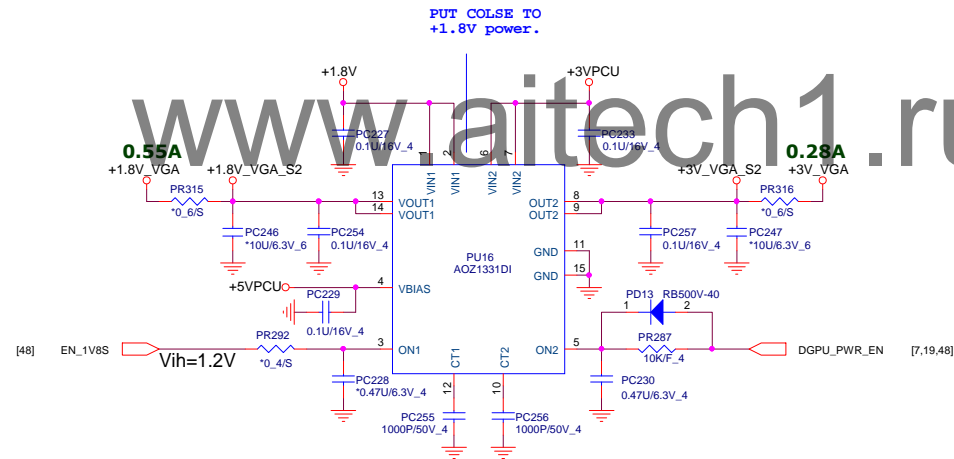
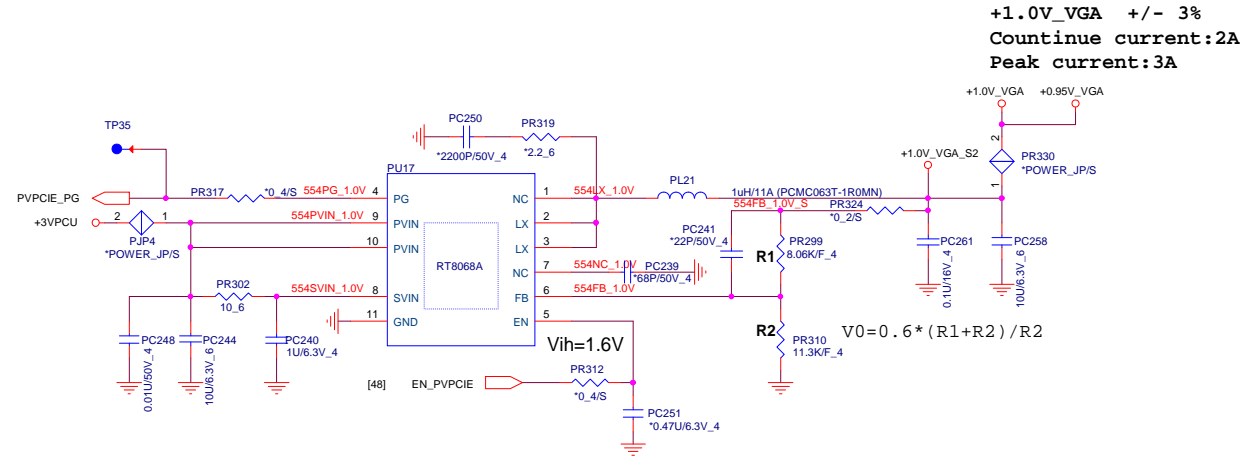
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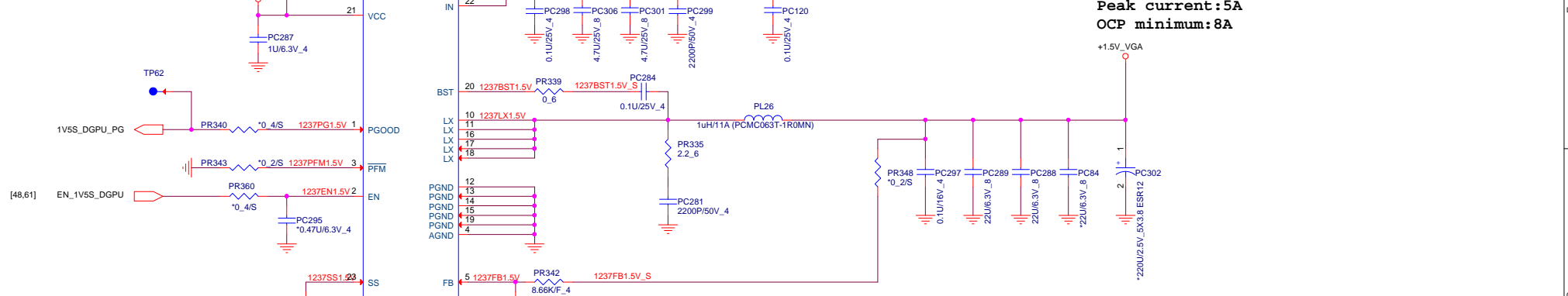




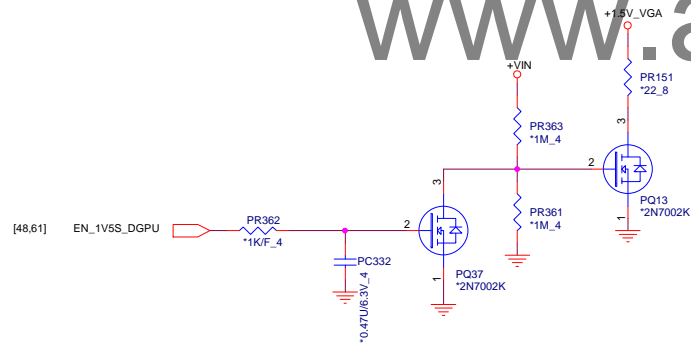
[www.aitech1.ru](http://www.aitech1.ru)



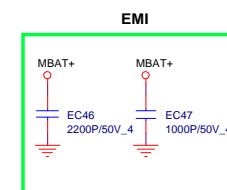
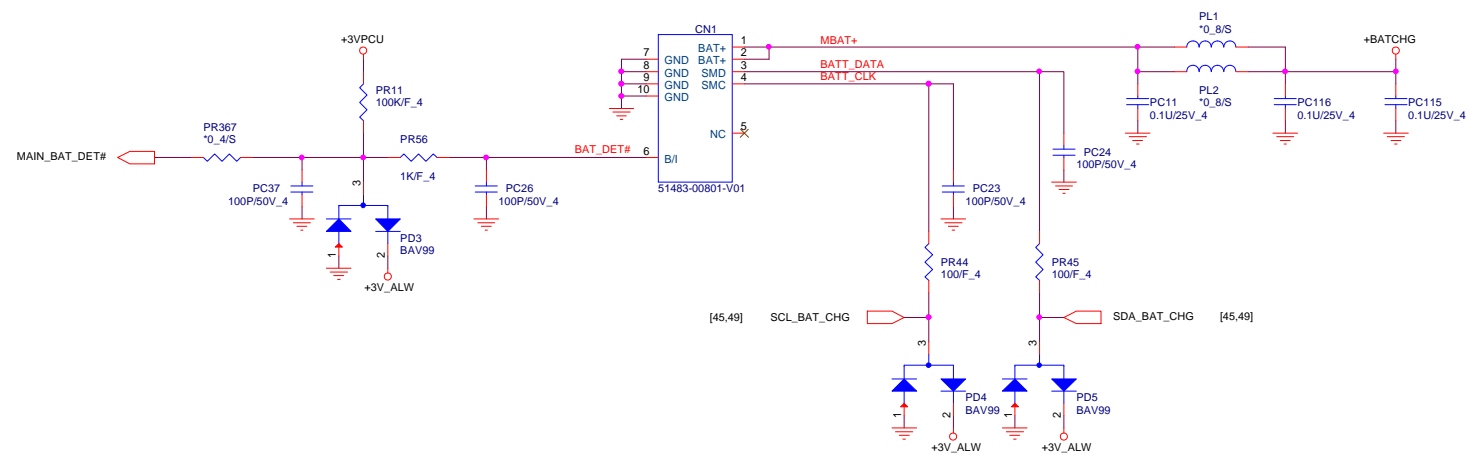
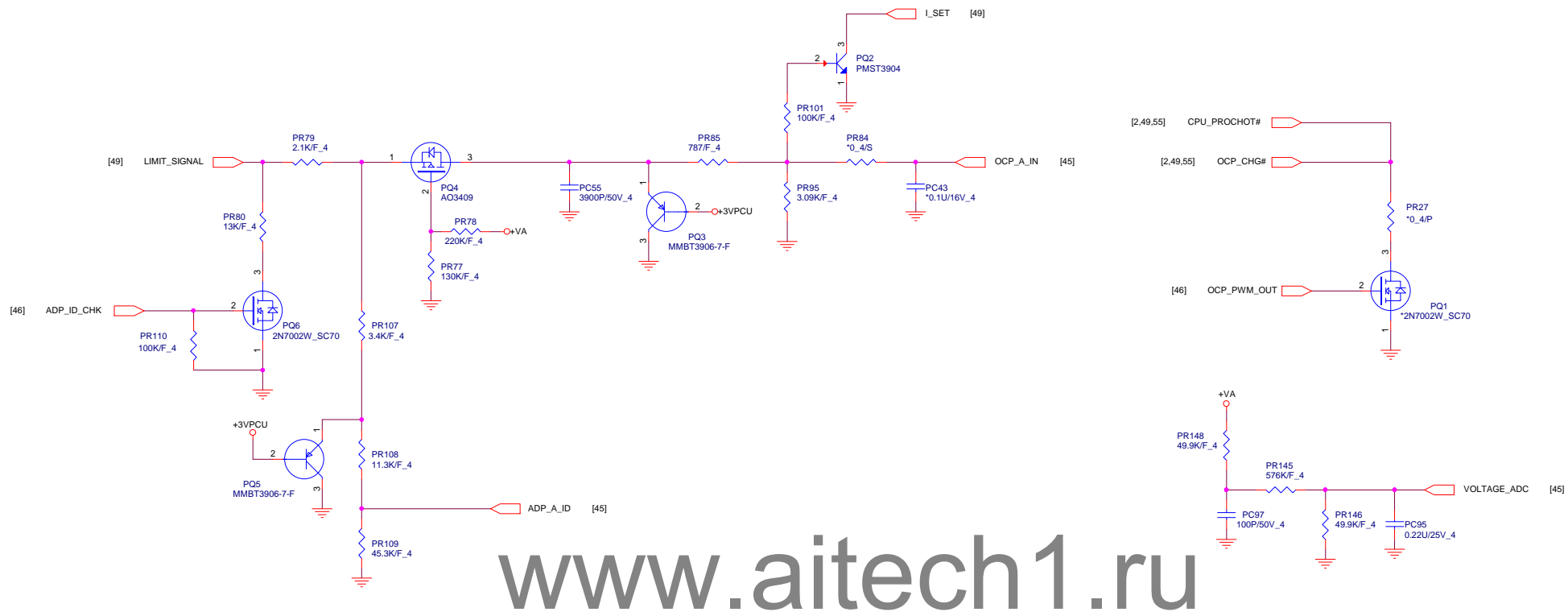




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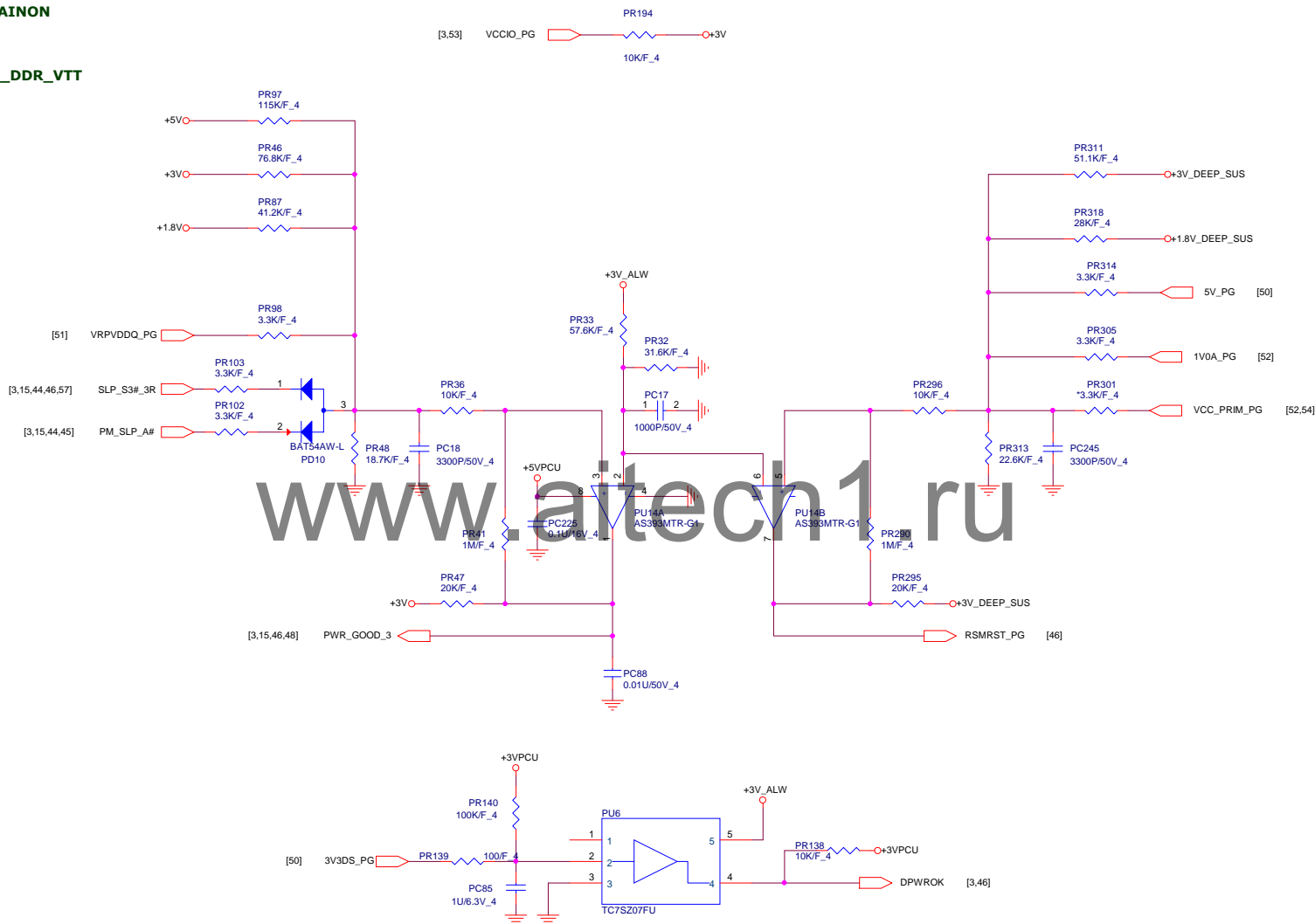


## Adapter OCP

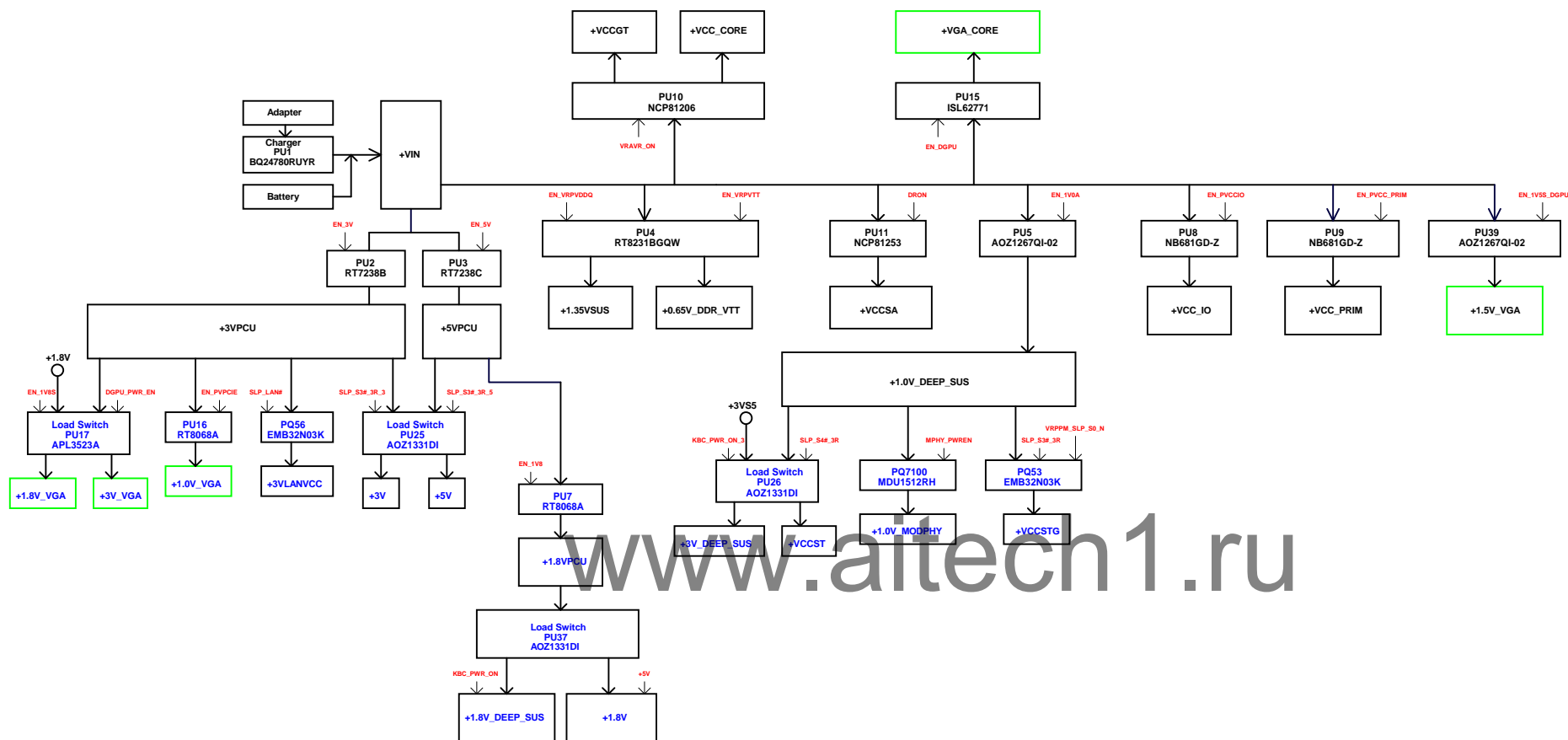


## POK CKT

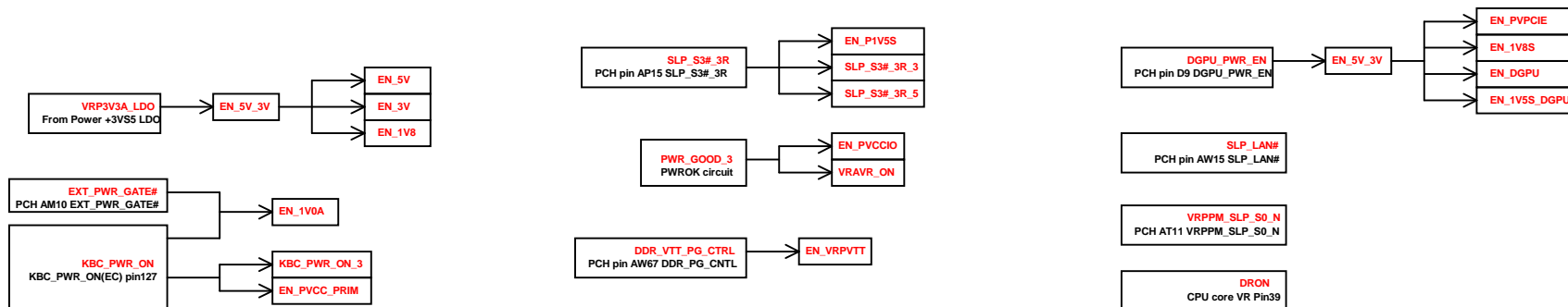
```
PM_SLP_S4# = SUSON
PM_SLP_S3# = MAINON
+V5S = +5V
+V3S = +3V
+V0.75S = +0.75V_DDR_VTT
```



## POWER BLOCK DIAGRAM

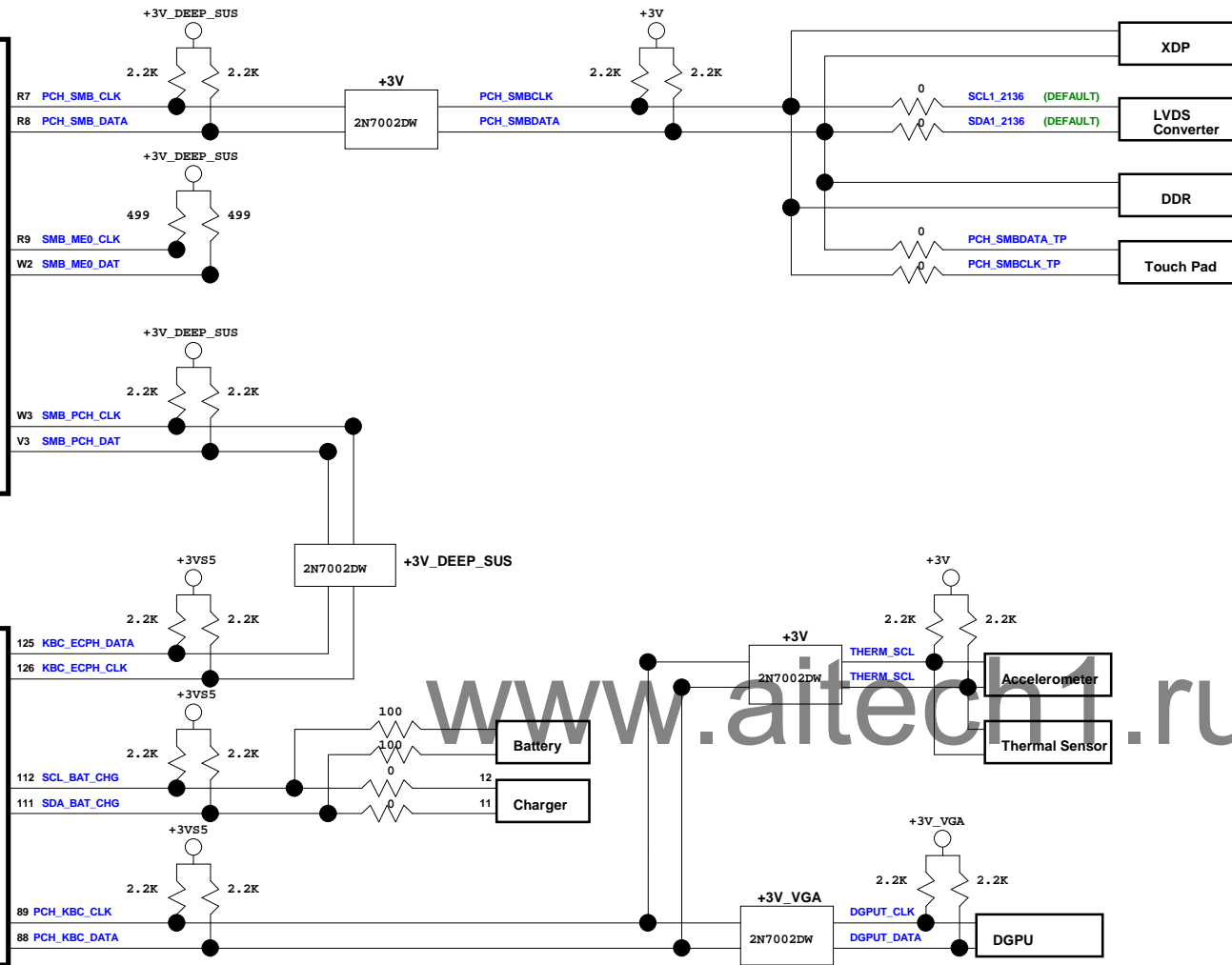


## POWER ENABLE PIN



SKYLAKE U

EC  
NPCE586H



Example: \*499/F\_4 and \*0\_6/S  
 \* means none-installed  
 499 means value  
 F means 1%  
 \_4 means 0402 size  
 /S means short pad

Multiplexed HSIO Lane	Port Assignment
USB3 #1	USB2.0/USB3.0 Combo Jack(Left side down)
USB3 #2 / SSIC #1	USB2.0/USB3.0 Combo Jack(Left side up)
USB3 #3 / SSIC #2	NC
USB3 #4	NC
PCIE1 / USB3 #5	dGPU
PCIE2 / USB3 #6	dGPU
PCIE3	dGPU
PCIE4	dGPU
PCIE5	LAN
PCIE6	WLAN
PCIE7 / SATA #0	HDD (SATA)
PCIE8 / SATA #1	ODD (SATA)
PCIE9	Cardreader (PCIE)
PCIE10	NC
PCIE11 / SATA #1*	NC
PCIE12 / SATA #2	SSD (SATA)

USB2.0	Port Assignment
USB2 #1	USB2.0/USB3.0 Combo Jack(Left side down)
USB2 #2	USB2.0/USB3.0 Combo Jack(Left side up)
USB2 #3	WWAN
USB2 #4	USB2.0(Right side on USB Board)
USB2 #5	USB2.0(Right side on USB Board)
USB2 #6	Touch Screen
USB2 #7	Bluetooth
USB2 #8	Finger Print
USB2 #9	Camera
USB2 #10	NC